Embedded Electronics for Intelligent Structures

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ABSTRACT

Intelligent structures with integrated control systems consisting of large numbers of distributed sensors, actuators, and processors have been proposed for the precision control of structures. This report examines the feasibility of physically embedding the electronic components of such systems. The hardware implications of functionality distribution are addressed, and it is shown that highly distributed systems can have substantially fewer communications lines and faster control loop speeds than conventional approaches, at the cost of embedding electronic circuit chips. A technique for the embedding procedure is presented which addresses electrical, mechanical, and chemical compatibility issues. Test specimens with functioning integrated circuits successfully embedded within graphite/epoxy composite laminates were subjected to static and cyclic mechanical loads, demonstrating nominal electrical function above normal design load limits. Operation of test specimens in a high temperature/humidity environement allowed the identification of a corrosive failure mode of the leads or lead-chip bonds. The application of a single-chip microcomputer to the control of a structural vibration problem demonstrates the potential for the development of monolithic integrated circuit devices capable of performing distributed processing tasks required for fully integrated intelligent structures.

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NOMENCLATURE

Chapter 2

A additions

B communication of a single bit

B_A communication of an address

B_D communication of a word of data

C number of chips

E equivalent operation

e vector of residuals

F_e, F_g residual, global feedback gain matrices

L number of lines

M finite element model mass matrix, multiplications

M_{gg} global block of transformed system mass matrix

N number of operations

n number of dof's in finite element model of system

N_C operations required for centralized control

n_e number of finite control elements

$N_{G/G}$ overhead performed by the global controller at the global rate

N_{GC} operations required for global control gains

$n_{g_{dof}}$ number of dof's per global node

n_{gn} number of global nodes

N_{GR} operations required at global loop rate

$N_{L/G}$ overhead performed by a local controller at the global rate

$N_{L/L}$ overhead performed by a local controller at the local rate

N_{LC} operations required for local control gains

N_{LR} operations required at local loop rate

P_C centralized control loop period

P_G global control loop period

P_L local control loop period

Q generalized forces in the finite element model

q vector of finite element model degrees of freedom

Q_e generalized forces in the finite element model due to residual feedback

Q_g generalized forces in the global model

q_g vector of global degrees of freedom

T number of communications operations

T_C communications operations required for centralized control loop

T_G communications operations required for global control loop

T_g interpolation matrix for global degrees of freedom

T_L communications operations required for local control loop

u vector of control inputs

ρ ratio of global loop period to local loop period

$(\,)_{I,\ldots,IV}$ option number

Chapter 3

E_L longitudinal elastic modulus

I_{DS} transistor drain-source current

V_{DS} transistor drain-source voltage

V_{GS} transistor gate-source voltage

Chapter 4

a compensator stage gain

b compensator pole frequency, compensator stage gain

D difference equation denominator coefficient

e_k compensator input sequence

$K(s)$ compensator design transfer function

$K_p(s)$ Pade time delay approximation

N difference equation numerator coefficient

s Laplace variable

u_k compensator intermediate state sequence

v_k compensator output sequence

z discrete transform variable

τ, τ_1 time interval between samples

τ_2 time interval between input and output

τ_p time delay due to discretization

CONTENTS

CHAPTER 1:
INTRODUCTION

Recently attention has been directed to the problem of precision structural control for such applications as flexible space structures [2,7,34,36] and high-performance robotics [4,8,28,35]. The demand for high performance control of rigid body modes alone tends to imply higher bandwidth requirements for the controller, which can begin to include the lower structural mode frequencies. A drive for lower weight also tends to lower the structural frequencies, increasing this overlap. The control problem thus becomes more likely to include structural vibrations, whether or not their control is explicitly specified.

Traditional thinking suggests that this be performed by a limited number of high authority actuators. This approach requires that the natural modes of the structure be known to a high degree of accuracy in order to provide high authority control of the controlled modes, yet avoid spillover into the modes not modeled by the controller [3]. Such an approach thus has fundamental limitations in terms of performance and bandwidth of control delivered. As the structure grows larger and more complex, its dynamic behavior becomes more difficult to predict. For a space structure, for example, ground testing becomes less feasible and less reliable; these difficulties lead can lead to on-orbit open loop behavior that differs substantially from pre-flight ground test measurements or analytical predictions.

A promising alternative to the traditional approach lies in the use of structures equipped with large numbers of highly distributed actuators and sensors. With such a system, software adjustments could be employed to

modify and tune closed loop behavior using the distributed sensors and actuators. This would allow superior control of individual flexible modes and would make the system less dependent on the precision of a priori knowledge of mode shapes. The ability to "fine tune" closed loop behavior is especially important when surface shapes and distances must be accurate to optical wavelengths, as is the case in adaptive optics. In addition, the distributed nature of the control system would allow continuous, hierarchical and impedance control algorithms to be implemented.

Systems with large numbers of distributed actuators and sensors such as these could benefit from similarly distributed and embedded processing electronics, yielding intelligent structures [33]. The distribution of electronic components could be used to exploit the computational benefits of parallel processing as well as to improve signal to noise ratios, and the embedding of these distributed components can simplify component interconnection. This distribution could also confer benefits due to increased robustness to component failure.

In a fully implemented intelligent structure, though, there is likely to be a substantial amount of circuitry to support the function of the actuators and sensors. Some sensors must be powered, and signals from the sensors must be conditioned and perhaps digitized. Actuators must be powered, and their driving signals switched. The control processing, either in analog, digital, or hybrid form, must also be performed by integrated circuits. All of these functions require distributed signal, power, and algorithm processing components.

Two possible options for the placement of these processing components are surface mounting and embedding, both of which have

advantages and disadvantages. Surface mounted components would offer ease of access and maintenance, but would be more easily damaged in service and would place functional demands on the structural surface which may conflict with existing requirements. Having components embedded within the structure could prove to be advantageous where structural surfaces must be kept "clean," e.g. in the case of a wing whose outer surface must be aerodynamically smooth and whose interior is occupied by fuel. Embedding components would also protect them from possible contact damage. A further advantage of embedding over surface mounting might be a reduction of the need to cut through many layers of a composite structure to connect the processing component to an embedded component such as a strain-based sensor or actuator.

It is the objective of this report to explore the possible advantages and feasibility of physically embedding electronic components for the control of intelligent structures. This will entail providing support for the contention that distributing and embedding components can confer advantages favoring intelligent structures over traditional approaches; demonstrating a method for embedding of electronic components in a composite structure; and demonstrating the plausibility of performing control tasks with circuitry implemented on a small number of chips.

Substantial work has been performed to date on embedding sensors and actuators in structures. In the area of mechanical control, the operation of strain actuators such as piezoelectrics and shape memory alloys has been demonstrated [12,30]. The analytic modelling and application of piezoelectric ceramics to the control of beam-like and plate-like structures in particular has received substantial attention, both in surface-bonded and embedded forms [11,13]. Among sensors, optical fiber schemes especially have been

investigated for use as distributed and embedded strain measurement sensors [29,32]. Such actuators and sensors could be surface mounted, or embedded in the intelligent structure.

Algorithms for the mechanical control of structures with large numbers of highly distributed sensors and actuators have also been developed. These range from high authority/low authority schemes [19], through more sophisticated hierarchic arrangements [21], to extremely decentralized and distributed wave or impedance based algorithms [15].

The problem of embedding electronic components specifically for the control of intelligent structures has received relatively little attention. The packaging issues involved, however, are similar in nature to those encountered during the original development of commercially practical resin-encapsulated integrated circuits [6]. Furthermore there exists at least one electronic device designed to operate within a composite part to monitor the resin state during the cure [5], providing a valuable starting point for the development of devices meant to withstand the cure and operate within a load-bearing composite structure.

The approach adopted in this report toward establishing the feasibility of embedded electronics for intelligent structures has three main aspects. To begin with, the potential advantages of a distributed, embedded control system must be supported. This is done by addressing the implications of distributing different levels of functionality and examining how this affects the resulting number of communications lines run into the structure, the number of chips required, and the computational load and speed of the control system. A comparison is drawn between a conventional centralized system and a hierarchic one which appears to naturally lend itself to

implementation in an intelligent structure.

The realization of a structure with a physically integrated control system requires the investigation of concerns about the integrity of the structure as well as the performance of electronics in a load-bearing structure. To this end, the various issues regarding electrical, mechanical, and chemical compatibility are examined, followed by the development of an embedding technique which addresses these issues and the selection of a test device to be embedded. A series of tests was performed to examine the performance of the embedded devices and explore possible failure modes. A number of devices were embedded in laminates which were cured and machined into test coupons. The effects of the inclusion on the structure and the functionality of the devices in the presence of stress were tested by subjecting a number of specimens to quasi-static and cyclic loads. The chemical isolation was investigated by subjecting other test articles to a high-temperature, high-humidity environment while under electrical bias to induce corrosion or other failures associated with moisture and ionic contamination. The test articles were carefully examined and the nature of the failure mechanisms was analyzed.

Once the basic feasibility of embedding electronics has been established, it remains to be shown that significant control tasks can be performed with a minimum number of chips. A microcomputer is identified which incorporates on a single chip many components (e.g., A/D and D/A conversion, high speed communication, memory) which are traditionally distributed among many separate chips. Closed loop control experiments on a piezoelectric-actuated cantilever beam were performed to demonstrate the capability of this single chip microcomputer in performing control tasks. It is apparent that a wide variety of functions can now be combined to greatly

reduce the number of chips required for a complete control system; combined with the ability to embed electronic components in general, this puts the development of true intelligent structures within reach. The presence of communication ports on these single chip microcomputers makes possible their incorporation into a network of such devices. This system could yield an efficient distribution of computational load, perhaps in the implementation of a hierarchic or decentralized controller.

In Chapter 2, the arguments for a distributed and physically integrated control system for an intelligent structure are presented. Chapter 3 addresses the electrical, mechanical, and chemical isolation issues involved in embedding electronic devices in composite structures, and describes the embedding technique developed and the results of mechanical and temperature/humidity/bias tests of the specimens manufactured with this technique. In Chapter 4, the functions of the single-chip microcomputer are described and the nature and results of the closed-loop control experiments are presented. Chapter 5 summarizes the results of the work, presents conclusions on the feasibility of embedding electronics for intelligent structures, and suggests directions for future work.

CHAPTER 2:
CONTROL ARCHITECTURE OF AN INTELLIGENT STRUCTURE

The elements of the control system of an intelligent structure range from the relatively abstract, such as the control algorithm, to the more concrete, such as the physical components which are used to implement the necessary functions. Between these two levels lies the communications system, the form of which is dependent on both the nature of the control algorithm and the characteristics of the physical components.

As suggested in Chapter 1, an intelligent structure with its large number of sensors and actuators can benefit from distributed control algorithms which differ from the centralized schemes traditionally applied to systems with relatively few sensors and actuators. The physical distribution of the functional components of the control system can also confer benefits.

The purpose of this chapter is to examine some of the possible architectures for the control of a structure with a large number of sensors and actuators. From the large number of possible control schemes, two will be selected for elaboration. These two will be used to contrast a distributed architecture with a traditional centralized one; a centralized feedback system will be compared with a hierarchic system which appears to lend itself to a high degree of functional distribution. For simplicity, the systems will be assumed to have available full-state information; output feedback would be a more realistic but unnecessarily complicating assumption. For both systems, the implications of physically distributing different levels of functionality of the control system components will be appraised. The effects of varying the

size of the control problem (i.e. the number of sensors and actuators) will also be considered, as will the implementation of different types of inter-level communication systems.

The many combinations of control scheme, level of functional distribution, and problem size could result in a large number of possible architectures. The evaluation of the two sample cases will be based on the essentially physical characteristics of the number of required communications lines and semiconductor chips, as well as achievable control loop speeds. More sophisticated measures of the performance capabilities of the various options are beyond the scope of this work, and will certainly depend on application to specific problems. Nevertheless it is hoped that the arguments presented in this chapter will provide some motivation for the development of intelligent structures with both distributed and embedded sensors, actuators, and processors.

In Section 2.1, some of the characteristics of the centralized and hierarchic control algorithms to be compared will be described, and a comparison of the numbers of operations required will be presented. This will be followed in Section 2.2 by an overview of the functions required by the control system and a discussion of the implications of the physical distribution of different levels of functionality. The chapter concludes with a comparison of the control loop speeds attainable with the two systems

2.1 Control Algorithms: Centralized and Hierarchic

Before examining the physical distribution of components and their location (i.e., embedded vs. non-embedded), we may briefly consider the implications of the overall control technique to be used. For the purposes of

this study, we will select for comparison two approaches to the functional arrangement of the calculations for the implementation of a state-space controller: centralized and hierarchic.. A centralized controller is one in which a single processor (computer) performs the compensation calculations, which might consist of optimal state feedback or an estimator with state feedback [25], or suboptimal output feedback [24,27]. A hierarchic controller uses processors arranged in two or more levels to perform these calculations [9].

In general, the better of two discrete-time control algorithms is the one which requires less time to perform a complete cycle or loop of control tasks, assuming the performance (in terms of some optimal cost of the continuous-time versions) is otherwise the same. In order to compare the centralized and hierarchic controllers in this section, the number of operations to be performed by each must be examined, along with the effective reduction due to execution, if any. A full time comparison must be postponed until Section 2.2.2, at which point the time required for data communication will have been investigated.

In the following discussion, the structure may be idealized as a finite element model in which measurements of all states are available through the distributed sensors at every nodal location, and in which forces are applied by means of the distributed actuators, as illustrated schematically in Figure 2.1. For a structure with n nodes, this would imply $2n$ sensors (giving both displacement and displacement rate) and n actuators. The availablity of all states naturally lends itself to a fixed-gain full-state feedback scheme. Control structures based on this approach will be considered sufficient for evaluation of the relative advantages and disadvantages of distribution, and the resulting conclusions should be applicable to some extent to more sophisticated

methods such as those involving output feedback or dynamic compensation.

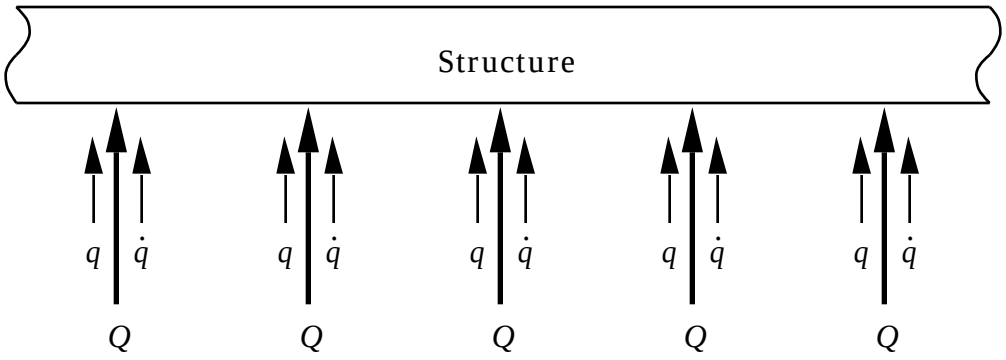

Figure 2.1 **Idealized structure with position (q) and rate ($\dot{q}$) sensors as well as an actuator (Q) at every node.**

2.1.1 Centralized Full State Feedback

The baseline comparison control algorithm structure will be assumed to be that of a centralized full-state feedback system [25]. This would essentially involve the multiplication of the vectors of all position and velocity measurements by full-rank gain matrices to yield the control forces to be applied at each actuator. The exact method used for the derivation of these gain matrices is not especially important, though a conventional choice might be the LQR technique [25]. This processing structure is illustrated in Figure 2.2,which shows the block diagram as well as the schematic of signal paths, the distributed sensors and actuators, and the single level of centralized processing.

For a centralized controller with a fixed gain control scheme such as LQR, the computation of the n actuator signals from the $2n$ sensor signals involves multiplication of a nx$2n$ matrix by a $2n$x1 state vector, resulting in N_C operations:

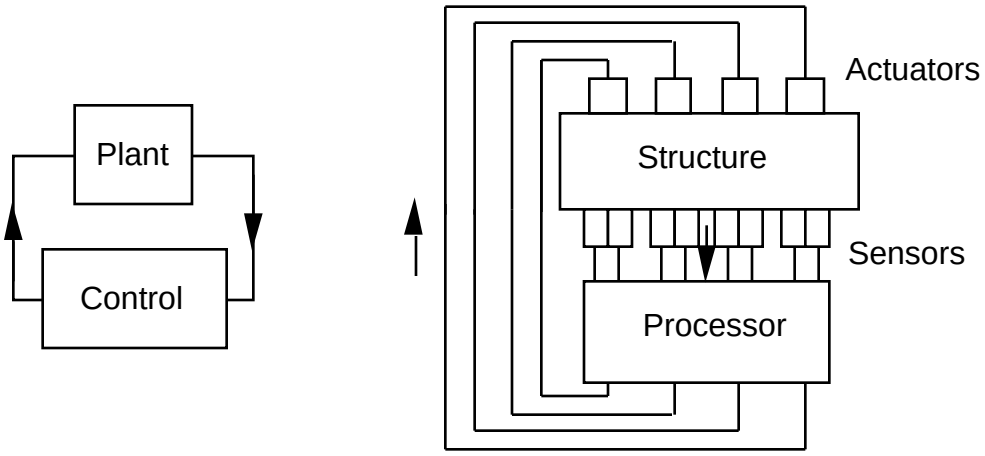

Figure 2.2 **Schematic of structure with centralized processing. Signal paths for a four-node system are shown on the right.**

$$N_C = 2n^2M + n(2n-1)A \\ \frac{1}{3}(8n^2 - n)E \tag{2.1}$$

In Equation (2.1), M and A refer to multiplication and addition, respectively; E is equivalent operation defined to be the same as one multiplication or three additions. This ratio is based on a comparison of the times required for the execution of the operations on a device such as the Intel 80C196KB single-chip microcomputer, described in more detail in Chapter 4. The proportionality of the computational load to the square of the number of nodes shows how quickly the burden increases with the size of the problem and, equivalently, with the number of sensors and actuators.

2.1.2 Hierarchic Control

In contrast to the centralized system, the hierarchic control system to be considered consists of two levels of processing, local and global, as proposed in [19, 21] and illustrated in Figure 2.3.

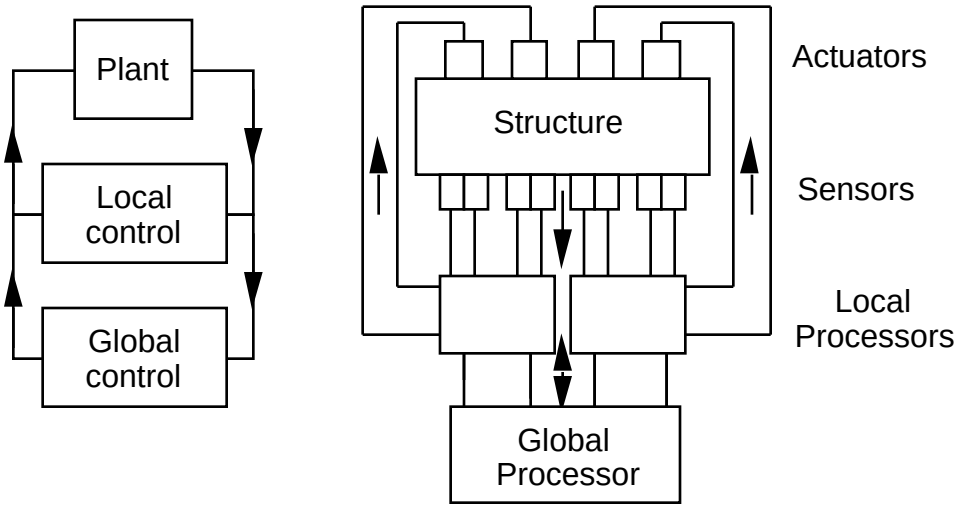

Figure 2.3 **Schematic of structure with hierarchic processing.**

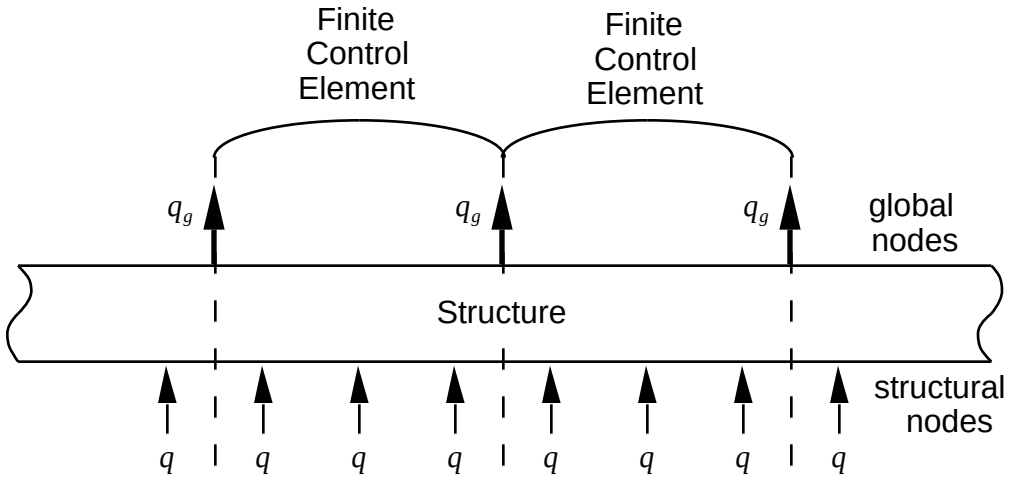

Figure 2.4 **Grouping of nodes into finite control elements. Structural (q) and global (q_g) displacements are shown; rates ($\dot{q}$, $\dot{q}_g$) and forces (Q, Q_g) are similarly grouped.**

The hierarchic controller described throughout this chapter is that developed by Hall *et al.* in [21] and described more fully by Howe in [22], from which much of the detail of the operations counts below has been drawn. This approach involves grouping the n nodes of the system and their associated degrees of freedom and generalized forces into n_e finite control elements (FCE's). This grouping is illustrated in Figure 2.4, in which the

FCE's have been formed from groups of three nodes. Each FCE is bounded on each side by a global node and has associated with it a local controller.

The computational tasks required for the implementation of this hierarchic control scheme are illustrated in the top block diagram of Figure 2.5. In the "o" (observation) loop, the local controllers condense the detailed state information $(q, \dot{q})$ from the sensors to yield a coarser description of the motion of the structure in terms of the state $(q_g, \dot{q}_g)$ of the $n_{gn}=n_e+1$ global nodes, each of which has $n_{g_{dof}}$ degrees of freedom. This last parameter can be used to determine in part the level of detail in the global model, and increasing it also increases the global computational load.

The global control forces Q_g are calculated from the reduced state information. The local controllers perform control calculations on the local residuals $(e, \dot{e})$, the difference between the actual nodal values and the values interpolated from the condensed global state model, to obtain Q_e. In the "c" (control) loop, any global component of Q_e is subtracted from Q_g, and the result is projected onto the full state system by the local controllers and added to the Q_e to produce u, the commands for the individual actuators.

The lower block diagram indicates the matrix multiplications required to execute these functions for a fixed-gain implementation. As described in [21], F_g and F_e are control gain matrices, T_g is the interpolation matrix, M is the mass matrix of the whole system, and M_{gg} is mass matrix of the global system model. It should be noted that the figure shows only the computations for the displacement states; a parallel "o" loop and residual and global control set of operations is required for the displacement rates.

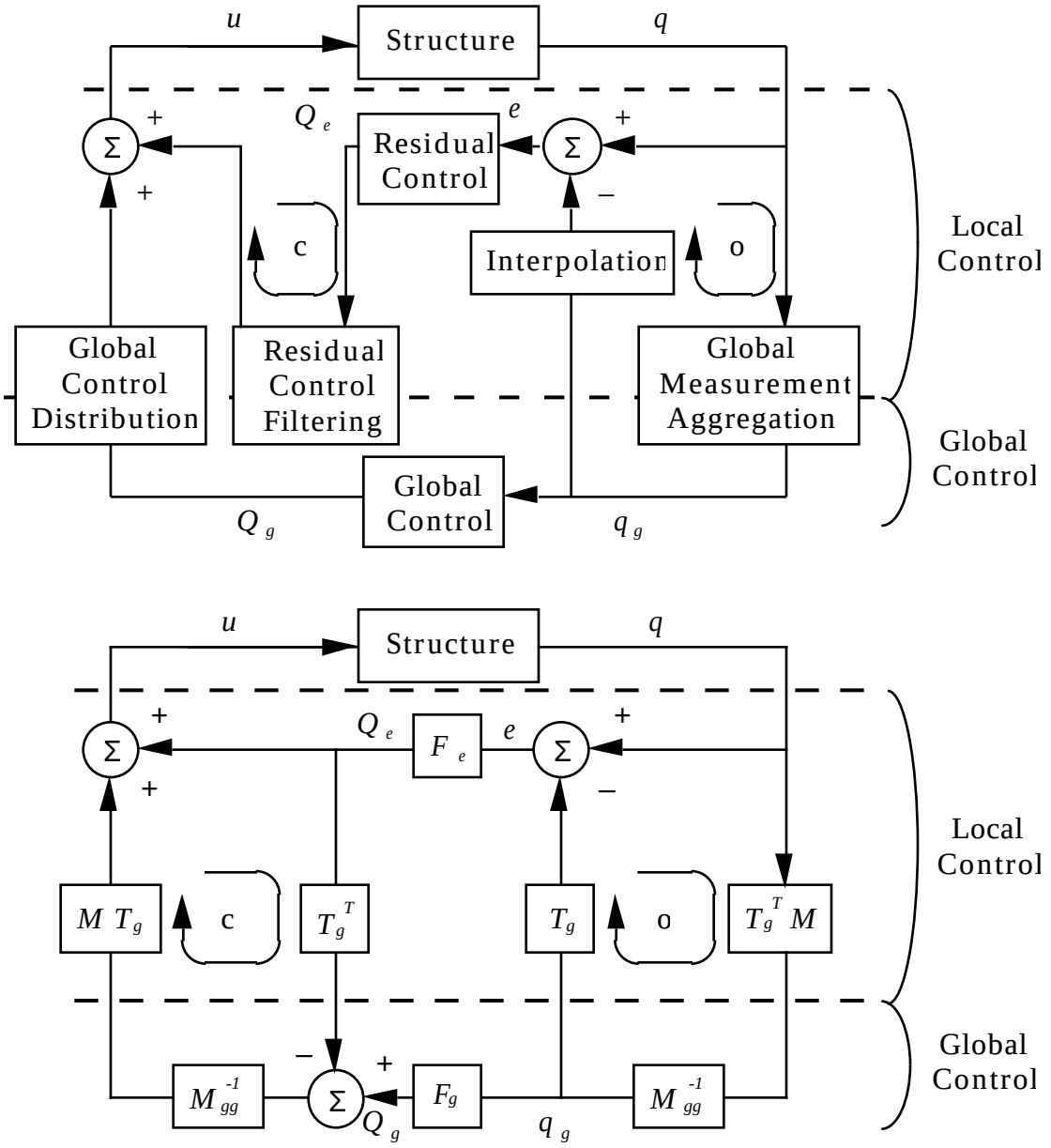

Figure 2.5 **Block diagram of the calculations required for the hierarchic control scheme. The parallel blocks for the rate computations ($\dot{q}$, $\dot{e}$, $\dot{q}_g$) are omitted for clarity.**

This arrangement thus defines two levels of control: the global level, in which a single controller is responsible for the overall deformation of the structure as reflected in the low frequency, long wavelength modes represented in the condensed state model; and the local level, in which a number of controllers each apply control forces within their own respective

domains, based on the measurements of the sensors within those domains.

The uniform, centralized system of the full-state feedback is thus replaced with a more segmented system, in which specific aspects of the nature of the problem are used to achieve greater computational efficiency. The grouping of local nodes into finite control elements mirrors the kind of grouping and condensation which is used in such structural analysis methods as component mode synthesis [10]. The response of the structure is naturally divided into lower frequency, long wavelength vibrations and higher frequency, short vibrations. The global controller acts on the former to control the overall deformation of the structure by using the condensed state description which omits unnecessary detail, while the local controllers act on the latter using only local information and applying only local forces, thus taking advantage of the high degree of spatial correlation of those motions.

The determination of the number of computations required for the hierarchic controller is substantially more complicated than for the baseline centralized controller. Not only are there more matrix multiplications than just the application of control gains, but the computations need not all be performed with the same frequency, and each local controller performs its tasks in parallel with the others. The hierarchic computation count will now be presented, starting with the application of the control gains at the global and local levels, and continuing with the additional overhead required for the "o" and "c" loops in Figure 2.5. Since each local controller runs in parallel with the others, all local computations may be represented by counting the computational load on a just one local controller.

The number of computations for the global controller required to compute Q_g from q_g and $\dot{q}_g$ is

$$N_{GC} = 2n_{g_{dof}}^2 (n_e + 1)^2 M + n_{g_{dof}} (n_e + 1)\left(2n_{g_{dof}} (n_e + 1) - 1\right) A$$
$$\frac{1}{3}\left(8n_{g_{dof}}^2 (n_e + 1)^2 - n_{g_{dof}} (n_e + 1)\right) E \qquad (2.2)$$

Assuming local control is performed using fully populated gain matrices at each local controller, the number of computations per local controller required to compute Q_e from e and $\dot{e}$ is

$$N_{LC} = 2\left(\frac{n}{n_e}\right)^2 M + \left(\frac{n}{n_e}\right)\left(2\frac{n}{n_e} - 1\right) A$$
$$\frac{1}{3}\left(8\left(\frac{n}{n_e}\right)^2 - \frac{n}{n_e}\right) E \qquad (2.3)$$

Comparing Equation (2.1) with Equations (2.2) and (2.3), it may be noted that $n_{g_{dof}}(n_e+1)$ and n/n_e appear in the latter two counts in the same way that n appears in the former. Examining the extreme limits for division into FCEs, it is apparent that when n_e =1, the resulting single local controller reverts to the centralized case and N_{LC}=N_C, while the global controller operations count N_{GC} shrinks to that of a vestigial two-node system. At the other extreme, where n_e=n-1, the local controller count N_{LC} becomes vestigial and N_{GC}=N_C if each node in the global model has one degree of freedom ($n_{g_{dof}}$=1), as do the nodes in the original, unreduced model.

Note that when n/n_e and $n_{g_{dof}}(n_e+1)$ are both less than n, the operations counts of Equations (2.2) and (2.3) will both be less than that of Equation (2.1). Since the local processors and the global processor in the hierarchic system are running in parallel, this suggests that both the local and global control can be performed faster than in the case of the centralized system. The local/global separation attained in the hierarchic system however entails a certain amount of overhead computation for the operations of the "o" and "c" loops shown in Figure 2.5; this overhead will now be accounted for.

The number of computations required of the global processor (performed at the global control rate) for the hierarchic interpolation, aggregation, filtering, and distribution functions is

$$\begin{aligned} N_{G/G} &= 3n_{g_{dof}}^2 (n_e + 1)^2 M + \left(3n_{g_{dof}}^2 (n_e + 1)^2 + n_{g_{dof}} (n_e - 5)\right) A \\ &\quad \frac{1}{3}\left(12 n_{g_{dof}}^2 (n_e + 1)^2 + n_{g_{dof}} (n_e - 5)\right) E \end{aligned} \tag{2.4}$$

The number of computations each local controller must perform at the global rate to support these overhead functions is

$$\begin{aligned} N_{L/G} &= 12 n_{g_{dof}} \frac{n}{n_e} M + 3\left(4 n_{g_{dof}} - 1\right)\frac{n}{n_e} - 2 n_{g_{dof}} A \\ &\quad \left(16 n_{g_{dof}} - 1\right)\frac{n}{n_e} - 2 n_{g_{dof}} E \end{aligned} \tag{2.5}$$

and the number required for each local controller at the local rate is

$$\begin{aligned} N_{L/L} &= 3\frac{n}{n_e} A \\ &\quad \frac{n}{n_e} E \end{aligned} \tag{2.6}$$

The total number of calculations performed at the global rate by the global controller and one local controller is then

$$\begin{aligned} N_{GR} &= N_{GC} + N_{G/G} + N_{L/G} \\ &= \left(5 n_{g_{dof}}^2 (n_e + 1)^2 + 12 n_{g_{dof}} \frac{n}{n_e}\right) M + \left(5 n_{g_{dof}}^2 (n_e + 1)^2 + 3\left(4 n_{g_{dof}} - 1\right)\frac{n}{n_e} - 12 n_{g_{dof}}\right) A \\ &\quad \left(\frac{20}{3} n_{g_{dof}}^2 (n_e + 1)^2 + \left(16 n_{g_{dof}} - 1\right)\frac{n}{n_e} - 4 n_{g_{dof}}\right) E \end{aligned} \tag{2.7}$$

and the total performed at the local rate by one local controller is

$$
\begin{aligned}
N_{LR} &= N_{LC} + N_{L/L} \\
&= 2\left(\frac{n}{n_e}\right)^2 M + 2\frac{n}{n_e}\left(\frac{n}{n_e} + 1\right)A \\
&\quad \frac{2}{3}\left(4\left(\frac{n}{n_e}\right)^2 + \frac{n}{n_e}\right)E
\end{aligned}
\tag{2.8}
$$

Taking $n_{g_{dof}}$=2, which would be the case for the global model of a beam which included position and angle at each global node, we find that Equation (2.7) becomes

$$
N_{GR} \quad \left(\frac{80}{3}\left(n_e + 1\right)^2 + 31\frac{n}{n_e} - 8\right)E \tag{2.9}
$$

In order to compare the computational load of the hierarchic system with that of the centralized system, some *ad hoc* assumptions are required. The number of FCEs (and hence local controllers), n_e, could be chosen to be

$$
n_e = \sqrt{n} \tag{2.10}
$$

so that the number of global nodes, n_{gn}=n_e+1 would be of the same order as n/n_e, the number of structural nodes per local controller. This choice could be refined based on arguments regarding the relative capabilities of the local and global controllers. The higher frequency of residual modes acted on by the local controllers would argue for fewer nodes per local controller and thus more FCEs, local controllers, and global nodes, and a larger, slower global control loop which would suffice for the slower nature of the global modes. Possible demands on the global controller to perform other tasks (such as control adaptation or damage assessment) would tend to reduce the desirable size of the global model, increasing the number of nodes per local controller and reducing the number of local controllers.

Using this assumption about the number of FCEs, Equations (2.9) and

(2.8) become

$$N_{GR} \quad \frac{1}{3}\left(80n + 253\sqrt{n} + 56\right)E \tag{2.11}$$

$$N_{LR} \quad \frac{2}{3}\left(4n + \sqrt{n}\right)E \tag{2.12}$$

The comparison of the centralized and hierarchic cases on the basis of computational load is somewhat problematic, especially since the two levels of hierarchic control operate in parallel and may operate at different rates. Neglecting the differing rates, we may separately compare the total number of operations in the centralized case, N_C in Equation (2.1), with the number performed at the global rate and at the local rate, N_{GR} and N_{LR} in Equations (2.11) and (2.12). This comparison is presented in Figure 2.6.

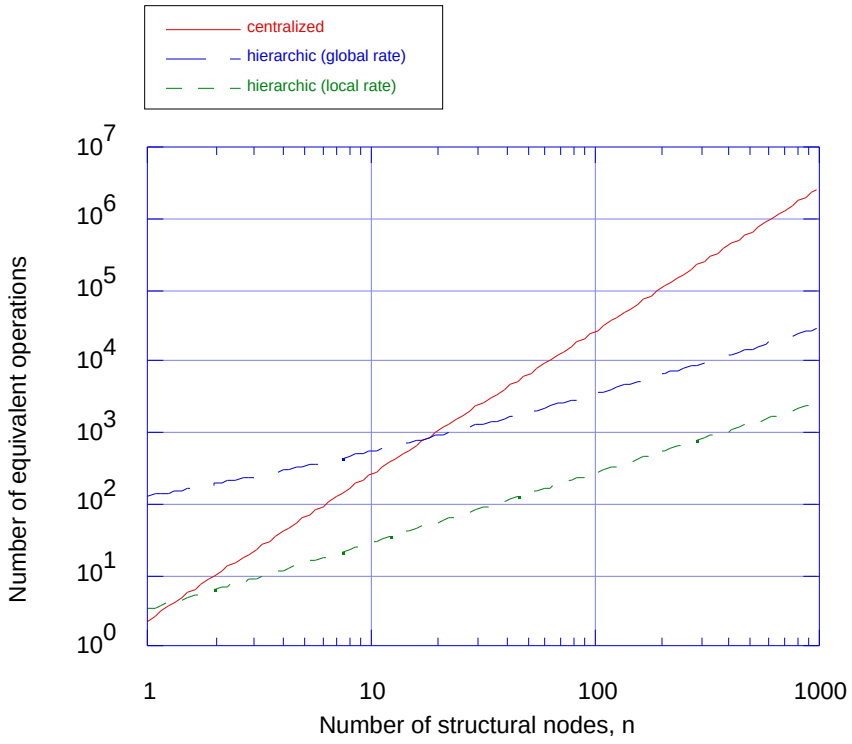

Figure 2.6 **Comparison of equivalent computations required by the centralized system and at the global and local rates of the hierarchic system.**

This figure can be interpreted in several ways. Comparing the

centralized and global rate curves, we see a crossover around 20 structural nodes, above which the global hierarchic control is less computationally intensive. This is to be expected, considering the $O(n^2)$ dependence of the centralized controller in Equation (2.1) and the $O(n)$ dependence of Equation (2.11). Of course, the global controller assumes a lower fidelity model of the structure, so the computational tasks performed at the local rate must also be considered. This curve also exhibits a dependence like $O(n)$ because of the particular selection of the number of local controllers. The computational load at the local rate per local controller is asymptotically only one-tenth that at the global rate. This suggests that many local control cycles could be completed for each global cycle. This would allow the previously described spectral separation, so that both the global and the local deformations would effectively be controlled based on models with appropriate levels of detail in the description of the shape, and at rates appropriate to their frequencies. This contrasts with the centralized system; in that case, in order to properly treat the short wavelength deformation, all computations would have to be performed at a high rate and the global modes would be described with unnecessary detail, resulting in a less efficient use of computational power.

The above examination neglects such questions as the performance degradation due to model reduction in the hierarchic system and the additional time penalty incurred by communication delays. The former issue is beyond the scope of this preliminary feasibility study, but is addressed at some length in [22], in which it is shown that the computational savings of the hierarchic algorithm can be achieved with only slight performance reductions as compared with the centralized system. The question of communication delays depends upon specific decisions regarding the means of data transfer among the various components of the control system, a

subject which is addressed in the following section.

2.2 Distribution of functionality

Having described two possible mathematical structures of the control algorithm, we now turn to the physical components required to implement the control. While the sensors and actuators themselves are assumed to be highly distributed, the other components necessary to implement the control may be distributed to a lesser or greater degree. The advantages of such a distribution might include improvements in signal quality, by locating conditioners near sensors; greater ease in handling large numbers of signals, by distributing the interfaces necessary for a digital bus; and increased control loop speed, by distributing processors operating in parallel throughout the structure.

This section will describe the required functions and examine the implications of different degrees of their distribution. A numerical comparison of various possibilities will be presented in terms of the numbers of required physical components such as circuit chips and conductor lines leaving the structure.

2.2.1 Required Functions

Regardless of the specific architecture chosen, certain functional components will be common to all the possibilities discussed here. These functions are shown schematically in Figure 2.7. At the lowest level, transducer elements are required for the sensing and actuation of physical variables; these might include strain gages and accelerometers on the sensing side and piezoelectric or electrostrictive materials on the actuation side. Both types of transducers will in general require some signal conditioning which

might include analog circuitry to obtain desirable sensor or actuator dynamics or to control noise, as well as signal and power amplification. This analog circuitry may be referred in general as analog processing.

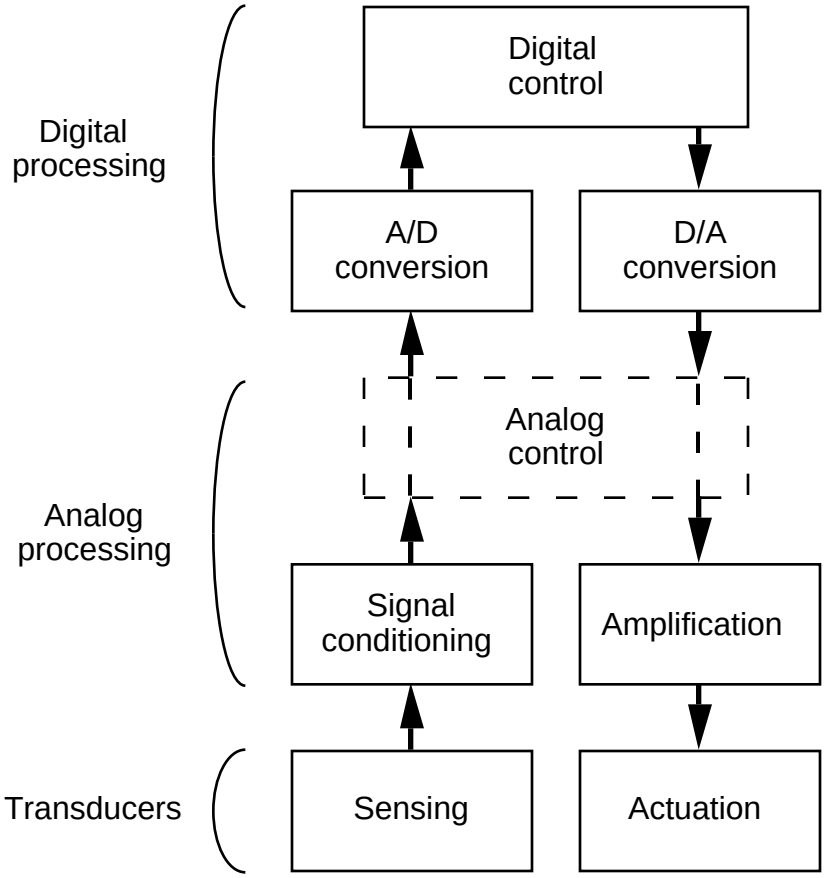

Figure 2.7 **Levels of functionality required for control system. Arrows indicate information flow.**

In order to take advantage of the flexibility of programmable digital processors for control, it is necessary to provide analog-to-digital (A/D) and digital-to-analog (D/A) conversion between the analog processing level and the digital control level. These blocks could also incorporate the necessary interface circuitry for a digital bus of some sort to transfer measurements and control commands. The highest functional block consists of the digital control itself, which, as described in Section 2.1, may or may not be divided

into hierarchic levels.

The very nature of the problem of controlling a structure requires that the transducer elements themselves be distributed about the structure, but many choices are possible regarding the distribution of the higher level components. Figure 2.8 presents four possible options for the distribution of the required functions of Figure 2.7. Functional components required for two structural nodes are shown, and the "edge" of the structure is indicated to show which functional components are distributed within the structure and the lines which must be run out of the structure. For the purposes of this analysis, a function is considered distributed only if the components which perform that function are themselves located in various places about the physical structure. All functions outside the structure are considered to be undistributed Distinctions of this kind, while in some ways strained and artificial when applied to a spectrum of engineering solutions, are nevertheless useful in sorting certain options within that spectrum.

The distribution of components introduces the requirement for a means of addressing them and allowing data transfer to and from them. The thin and thick lines in Figure 2.8 represent two different types of electrical connection of components. The thin lines show analog connections: dedicated signal lines carrying continuous voltage representations of the data, with addressing implicit in the dedicated nature of the lines. The thick lines indicate digital buses, in which data are represented by discrete voltage levels on common conductor lines. This requires the presence of the A/D and D/A conversion, as well as some kind of digital interface circuitry, which is assumed to be included on the blocks labeled A/D and D/A.

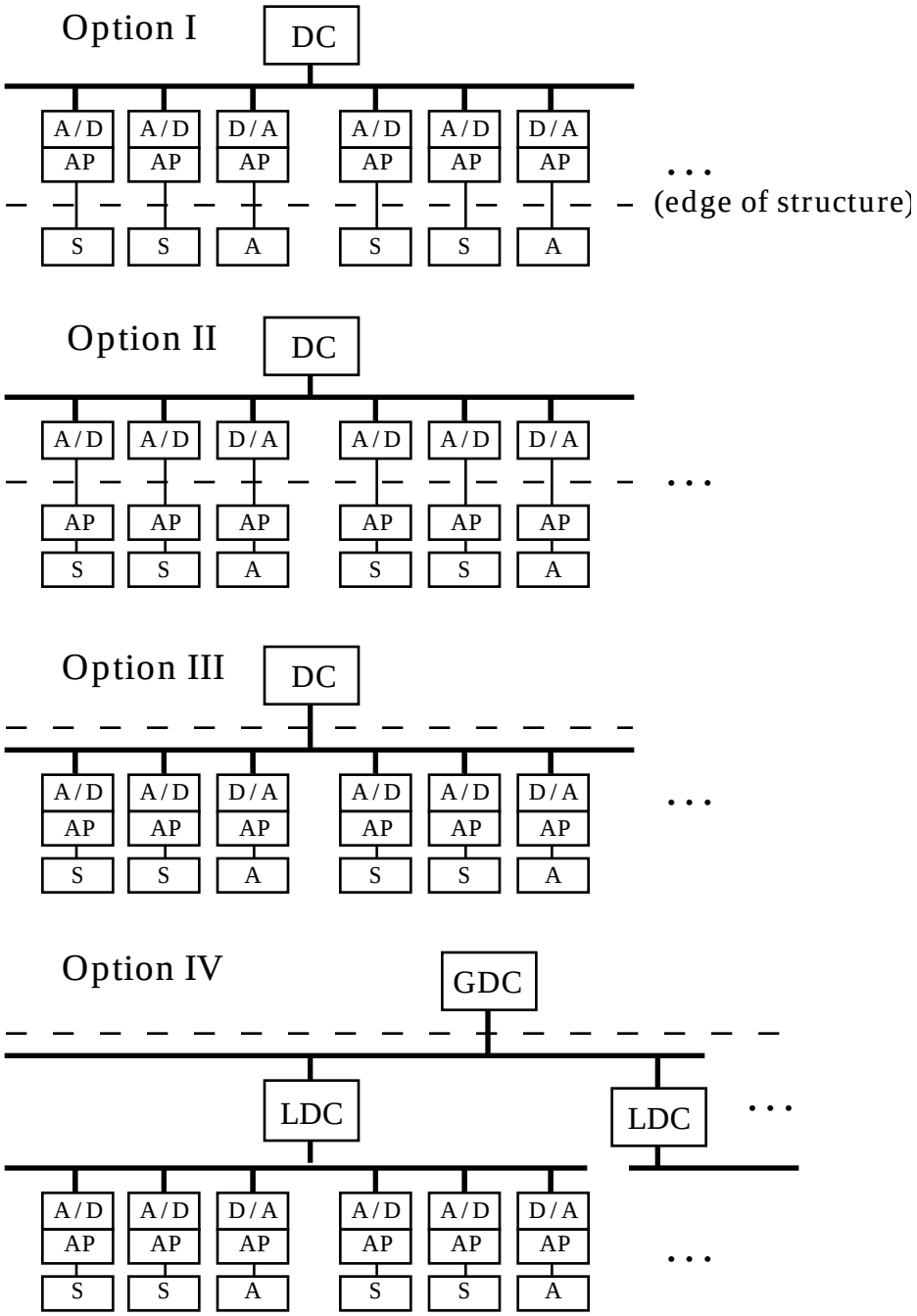

Figure 2.8 **Four options for distributing functionality. DC=digital computer, AP=analog processing, S=sensor transducer, A=actuator transducer, GDC=global digital computer, LDC=local digital computer.**

Option I corresponds to the conventional approach, in which the transducers alone are distributed, and the connections to them are of analog form. In option II, analog processing has been distributed along with the

transducers, but communication between distributed and non-distributed components is still by means of analog lines. In option III, A/D and D/A conversion has also been distributed, allowing a digital bus to be used for connecting the distributed components.

Option IV assumes a hierarchic controller of the type described in Section 2.1.2. This option incorporates distributed digital control in the form of local computers, which communicate with the external global controller by means of a digital bus. Communication between local computers and lower level functional components is shown as a digital bus, but this could be arranged differently; digital conversion and analog processing could be combined on the same chip as the local computer, resulting in analog connections for the local groups. As stated earlier, though, only those conductor lines leaving the structure are being considered here. The hardware implications of these four options will be described in the next section.

2.2.2 Hardware Implications of Functional Distribution

A preliminary analysis of the effects of various degrees of distribution of the required functionality may be performed on the basis of the number of chips required to perform those functions and the number of conductor lines which must enter the structure to connect the distributed components with those not distrubuted. A rationale for estimates of the number of chips and lines will be developed, and comparisons will be made among the results for levels of distribution. The cases to be considered are the four options described in Section 2.2.1, and illustrated schematically in Figure 2.8.

In option I, the case in which only the transducer elements themselves are physically distributed over the structure, the number of distributed

integrated circuit chips is evidently zero. We may assume that each transducer would require two conductive lines; one to carry the signal and one to act as a ground reference. This would suffice for a strain gage or other sensor forming part of a balanced bridge, or for an actuator such as a piezoceramic. If there are n nodes, and one actuator and two sensors per node (one sensor for displacement and one for rate), the number of distributed chips C and the number of lines entering of the structure L may be estimated for option I to be

$$\begin{aligned} C_I &= 0 \\ L_I &= 3n + 2 \end{aligned} \tag{2.13}$$

assuming that two grounds are provided, one for all sensors and one for all actuators. This could be conservative, as each transducer might require a few additional lines (e.g. dedicated ground or excitation lines), but the number of lines is in any case likely be roughly equal to a small multiple of the number of structural nodes.

In option II, analog processing chips are distributed to avoid the corruption of low level signal over long lines by performing signal conditioning and amplification near each transducer. For simplicity, the possibility of analog control (see Figure 2.7) involving interconnection of nearby sensors and actuators is neglected. Each sensor transducer might be driven and its signal buffered by a single chip with analog circuitry, and a similar provision could be made for amplifying the signal to each actuator transducer. If we assume that all analog circuit chips require common positive and negative low level voltage supplies (perhaps 5 or 12 volts), and that the actuator amplifiers may require positive and negative high voltage supplies, we must add four more lines entering the structure, as well as a chip for each transducer element, so that the counts for this option are

$$C_{II} = 3n$$
$$L_{II} = 3n + 6 \qquad (2.14)$$

In option III, the unwieldy number of conductor lines in systems with many sensors and actuators is avoided by means of a digital bus. This requires the distribution of A/D and D/A conversion functions, as well as a bus interface capability. Assuming that the digital conversion and interface functions can be combined with the analog processing on a single chip (indicated in Figure 2.8 by the contact of the blocks for conversion and analog processing), the total number of chips is the same. The six power and ground lines also remain unchanged, but the dedicated signal lines to each transducer are replaced by the lines required for the bus, the nature of which will now be briefly considered.

The number of bus lines depends on the type of bus implemented, parallel or serial. A common example of a parallel bus is the IEEE 488 standard [23]. In this type of bus, information is transmitted by making the voltages on several conductor lines simultaneously correspond to the values of the bits in a word of data, often an 8-bit byte or a two byte word. Additional control lines are used to coordinate the transfer between devices in a process known as handshaking. One line is used by the master device to indicate to the slaves that the information present on the data lines is valid (i.e., the voltages have settled). Two other control lines carry handshaking signals back from the slaves to the master; one to signal readiness to accept information and one to acknowledge that the information has been received.

The selection of the device desired for data transfer, or addressing, is accomplished in the IEEE 488 with the same lines which carry data, along with an additional control line to indicate whether the information present on the parallel lines is an address or data. A bus which uses the same lines

for carrying data and addressing information in this way is said to be multiplexed. The structure of the both the centralized and hierarchic controllers described in Section 2.1 is sufficiently well-defined that an explicit indication of the direction of data transfer is not necessary.

The number of data lines depends on the number of devices to be addressed and on the size of the unit of data to be transmitted in parallel. If there are k devices to be addressed, $[\log_2 k]$ lines are required, where [ ] indicates the least integer function. We can assume a minimum of 8 such lines as in the IEEE 488, so that one 8-bit byte at a time may be transferred. The IEEE standard further calls for a single ground for all data lines and separate grounds for the four control lines. To these we must add the 6 power and ground lines identified in option II, as well as a clock signal required by all finite state devices.

Another possibility for the digital bus would be a serial bus, which typically consists of one or two lines for signals and a ground return. To these are added the control lines and their grounds, as well as the usual power and ground set and a clock line. The total number of lines for a serial bus would then be 13. The reduction in lines achieved by using a serial bus instead of a parallel bus is not nearly as noticeable as that achieved using a parallel bus instead of analog connections. For this reason, and because the slow speed of serial buses tends to make them unsuitable for real-time control of fast processes, the buses in options III and IV will be assumed to be of the parallel type.

In view of these considerations, we find that option III results in the following chip and line counts:

$$\begin{aligned} C_{III} &= 3n \\ L_{III} &= 16 + \max\left(8, \lceil \log_2 3n \rceil\right) \end{aligned} \tag{2.15}$$

Note that the number of chips required remains the same since it has been assumed that digital and analog circuitry can be implemented on a single chip.

In option IV, some portion of the digital control itself is distributed in the form of the local controllers in order to take advantage of the faster control loop speeds which the operations count discussion of Section 2.1.2 suggested were possible with the hierarchic system. The global controller communicates with the n_e local controllers by means of a parallel bus. Assuming the local controllers to be implemented as single-chip microcomputers, the number of distributed chips would increase somewhat to

$$\begin{aligned} C_{IV} &= 3n + \sqrt{n} \\ L_{IV} &= 16 + \max\left(8, \frac{1}{2}\log_2 n\right) \end{aligned} \tag{2.16}$$

where the number of local controllers has again been determined by assuming $n_e = \sqrt{n}$.

The numbers of chips and lines as a function of level of distribution in options I-IV, Equations (2.13)-(2.16), are summarized in Table 2.1.

Table 2.1 **Numbers of communications lines and distributed circuit chips for different levels of distributed functionality.**

Highest Level of Distributed Functionality	Number of chips	Number of lines
Option I (transducers)	0	$3n+2$
Option II (analog processing)	$3n$	$3n+6$
Option III (digitization)	$3n$	$16+\max\left(8,\lceil \log_2 3n \rceil\right)$
Option IV (digital control)	$3n+\sqrt{n}$	$16+\max\left(8,\left\lceil \frac{1}{2}\log_2 n \right\rceil\right)$

An examination of the results summarized in this table shows some of the trades encountered in the decision of the desirable level of functionality distribution. Distributing analog processing (option II) could improve signal to noise ratios at the cost of a small increase in the number of conductor lines and a number of chips proportional to the number of structural nodes. If the presence of those chips is supportable, however, a substantial savings in terms of lines can be obtained by distributing digital conversion and bus interface functions as well (option III). This savings reduces the dependence of the number of lines from *O(n)* to *O*($\log_2 n$) which could be very important for systems with large numbers of sensors and actuators.

The distribution of the digital control in option IV does not appear in the table to yield much if any advantage except when the system is so large that the $[\log_2 3n]$ is large compared to $[\frac{1}{2}\log_2 n]$. The real benefits of this option are to be found in the comparison of control loop speeds achievable with undistributed and distributed computational power. The number of

equivalent operations required for the centralized and hierarchic control algorithms has been presented in Section 2.1; to derive loop time comparisons, the time required for these computations must be calculated and added to the time required for data transfer. Additional time is required for A/D and D/A conversion, but as this is the same in all cases, it will be neglected.

The computational load counts of Section 2.1 are expressed in terms of equivalent operations, each representing one multiplication or three additions. For a single-chip microcomputer like the Intel 80C196KB used in the control experiment of Chapter 4, an equivalent operation takes approximately 20μs. A more powerful processor would be faster, but the use of this single number will suffice for the purpose of comparing the two algorithms. The limits on the speed of data transfer on digital buses depends substantially on the details of propagation delay on conductor lines, line termination conditions, and driver and receiver characteristics. For the purposes of this study, a parallel bus data transmission rate of 100000 bits/s will be assumed.

The number of data transfer operations associated with one control loop by the centralized controller of option III is given by

$$\begin{aligned} T_C &= 3nB_A + 3nB_D \\ &= 3n(B_A + B_D) \end{aligned} \tag{2.17}$$

where B_A and B_D represent an address and a data transfer, respectively. $3n$ transfers are required since each of the n nodes has two sensors and one actuator. If we assume that an address consists of 8 bits ($B_A = 8B$) and a word of data consists of 16 bits ($B_D = 16B$), we get

$$T_C \quad 72nB \tag{2.18}$$

We can now compute the time required for the centralized controller in the configuration of option III to complete one control loop. Combining Equations (2.1) and (2.18) we find the period of the centralized controller loop to be

$$\begin{aligned} P_C &= N_C + T_C \\ &\frac{1}{3}\left(8n^2 - n\right)E + 72nB \\ &\frac{1}{3}\left(8n^2 + 107n\right)E \end{aligned} \tag{2.19}$$

where in the final line we have made use of the assumptions that an equivalent operation is of 20μs duration and that the bus speed is 100000 bits/s, so that transmitting one bit requires 10μs or half an equivalent operation.

In obtaining the control loop period estimates for the hierarchic system (option IV), both the global and local computations and data transfers must be considered. First, Figure 2.5 shows that a complete global loop involves four transfers of data between the global and each local controller, two transfers each for the "o" and "c" loops. Each of these transfers entails an addressing operation. The "c" loop transfers also involve a word of data for a force component for each of the $n_{g_{dof}}$ global degrees of freedom in the FCE, and the "o" loop transfers involve one word of data for a displacement and one for a displacement rate for each of the $n_{g_{dof}}$ global degrees of freedom in the FCE. The total number of data transfer operations for one complete global loop is

$$\begin{aligned} T_G &= \left(4B_A + 12n_{g_{dof}}B_D\right)n_e \\ &416\sqrt{n}B \end{aligned} \tag{2.20}$$

where the previous assumptions regarding the number of FCEs $n_e=\sqrt{n}$, the length of addresses and data, and the number of degrees of freedom per global node $n_{g_{dof}}=2$ remain in force. To these data transfer operations we must add

the equivalent operations for the control and overhead calculations, as given by Equations (2.2) and (2.4), to get the global loop period

$$\begin{aligned} P_G &= N_{GC} + N_{G/G} + T_G \\ &\quad \frac{1}{3}\left(32n + 62\sqrt{n} + 30\right)E + \frac{1}{3}\left(48n + 98\sqrt{n} + 38\right)E + 416\sqrt{n}B \\ &\quad \frac{1}{3}\left(80n + 784\sqrt{n} + 68\right)E \end{aligned} \tag{2.21}$$

The determination of the period of the local loop is somewhat more complicated, as each local controller must perform some overhead calculations at the global loop rate rather than the local loop rate. This means that if we let ρ be the number of local loops performed during each global loop so that

$$P_G = \rho P_L \tag{2.22}$$

then each local controller must perform its local rate computations (N_{LC}, $N_{L/L}$ from Equations (2.3) and (2.6)) and local data transfers (T_L) ρ times during the global cycle, as well as its global data transfers and global overhead computations:

$$P_G = \rho\left(N_{LC} + N_{L/L} + T_L\right) + \frac{1}{n_e}T_G + N_{L/G} \tag{2.23}$$

so that the loop period ratio is

$$\rho = \frac{P_G - \frac{1}{n_e}T_G - N_{L/G}}{N_{LC} + N_{L/L} + T_L} \tag{2.24}$$

Local data transfer is similar in form to that of the centralized controller:

$$\begin{aligned} T_L &= 3n_e B_A + 3n_e B_D \\ &= 3n_e\left(B_A + B_D\right) \\ &\quad 72\sqrt{n}B \end{aligned} \tag{2.25}$$

Combining the results from Equations (2.3), (2.5), (2.6), (2.20), (2.21), (2.24), and (2.25) and simplifying, we find that

$$\rho \quad \frac{\left(80n + 67\sqrt{n} + 80\right)E + 1248\left(\sqrt{n} - 1\right)B}{\left(8n + 2\sqrt{n}\right)E + 216\sqrt{n}B}$$

$$\frac{80n + 691\sqrt{n} - 544}{8n + 110\sqrt{n}} \tag{2.26}$$

Figure 2.9 shows the periods (expressed in terms of equivalent operations) of the centralized, global, and local loops as a function of the number of structural nodes. We see that under the given assumptions, the local loop of the hierarchic system becomes faster than the centralized system loop for systems with more than 3 nodes, and a similar crossover occurs for the global loop of the hierarchic system at about 20 nodes. The period of the local loop asymptotes to 1/10 that of the global loop, so that ρ approaches 10, as would be expected from the computation counts given in Section 2.1.2 in Equations (2.11) and (2.12) and plotted in Figure 2.6. The data transfer loads from Equations (2.20) and (2.25) are of order $\sqrt{n}$, while the computational loads are of order n, so that computation dominates for large systems. For small n, the global communications requirements tend to load the local systems more heavily than for large n, making r smaller and producing the initially elevated local loop periods apparent in Figure 2.9.

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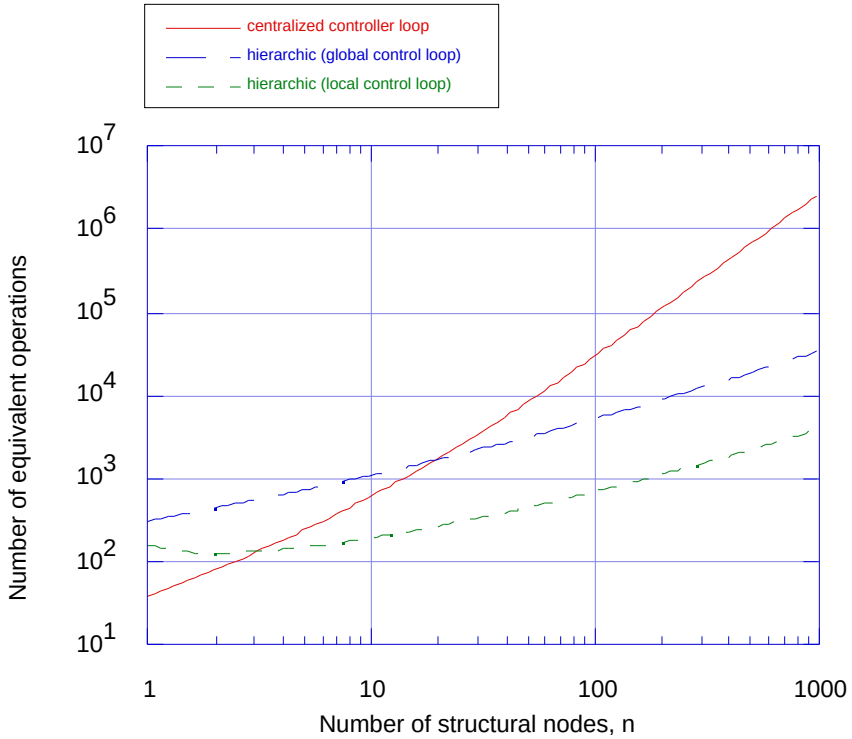


Figure 2.9 **Comparison of equivalent operations required by three control loops: the centralized system and global and local loops of the hierarchic system. Data transfer and computation loads are both included.**

(2.11) and (2.12) and plotted in Figure 2.6. The data transfer loads from Equations (2.20) and (2.25) are of order $\sqrt{n}$, while the computational loads are of order n, so that computation dominates for large systems. For small n, the global communications requirements tend to load the local systems more heavily than for large n, making r smaller and producing the initially elevated local loop periods apparent in Figure 2.9.

If we examine the particular case of a problem with n=100 structural nodes, we can apply Equation (2.19) find that the period of the centralized control loop is 605ms, 88% of which is due to computational load. Applying hierarchic control to the same problem, we find from Equations (2.21), (2.22), and (2.26) that the period of the global loop is 106ms (61% computation) and that of the local loop is 14ms (45% computation). The global hierarchic loop

in this case is 5.7 times faster than the centralized loop, and the local hierarchic loop is 7.6 times faster than the global loop and 43 times faster than the centralized loop.

The advantage of the hierarchic control of option IV over the centralized control of option III is thus apparent. The reduction in the number of operations achieved by model reduction and parallelism, as presented in Section 2.1, results in a system which can execute even a global loop faster than the centralized controller, and can execute a local loop still faster.

CHAPTER THREE:
FEASIBILITY OF EMBEDDING ELECTRONIC COMPONENTS IN GRAPHITE/EPOXY COMPOSITES

In the previous chapter arguments were presented that suggested the advantages of physically embedding electronic components of control systems in structural elements to form intelligent structures. The application of this proposed technology to the solution of an actual design problem presupposes the capability of performing the embedding. The purpose of this chapter is to examine issues regarding the feasibility of embedding and to describe an attempt to develop and demonstrate the basic embedding capability, as well as efforts to identify basic failure modes with an eye toward future technique modifications.

This chapter begins with a discussion of the general issues expected to be of concern in embedding electronic devices. Remarks regarding the selection of a specific test device to be embedded are then followed by a description of the device and the technique developed for embedding it in graphite/epoxy laminates. The manufacture of the test articles is then detailed, and the tests performed on them are described. Finally, the results of these tests are presented.

3.1 Overview of Major Issues and Technique

The problem of embedding electronic components in structural materials can be addressed both from the point of view of a structural engineer interested in ensuring mechanical performance and integrity in the presence of non-structural inclusions, and from that of an electrical engineer

concerned about the mechanical, electrical, chemical, and other effects of the surrounding structure on the behavior of the electronic devices. While this work is primarily concerned with the survival of the embedded devices, basic structural issues must be addressed first. These considerations will lead to the selection of an appropriate form of packaging for the electronic devices to be embedded.

The overriding structural principle must be to keep both the number and size of such inclusions to a minimum, as they are likely to decrease the effective elastic modulus of the material and induce stress concentrations. Such concentrations could serve as sites for the beginning of delaminations and cracks, leading to premature structural failure of the component. Clearly electronic devices with some kind of minimal packaging are desired which, when embedded, present the smallest possible interruption to the fewest possible number of plies of the composite.

Such a minimal packaging is available in the form of tape automated bonding (TAB). This is a procedure developed to simplify the connection of metal leads to the bonding pads of silicon chips bearing integrated circuits requiring high numbers of such connections [18]. In commercial applications of TAB, leads are patterned by photolithographic means and the etching of a metal foil affixed to a polymer carrier tape with frames and sprockets, much like movie film. The ends of the leads which extend into an open window punched in each frame of the tape are all simultaneously attached to the corresponding bonding pads on the chip. The chips on the carrier tape assembly then proceed through further packaging steps, often involving encapsulation in plastic or a hermetic metal container and mounting on a circuit board.

The TAB assembly itself, though, has all the necessary electrical connections for electrical operation, and is not much larger than the chip itself. The required interconnections with other chips or with sensor or actuator elements could be formed by extending the length of the leads using flexible circuits for cables. By eliminating the conventional encapsulation steps, a functioning electronic part is obtained which, by virtue of its small profile, would cause minimal interruption of the plies of the composite in which it is to be embedded.

While the small profile achieved by the use of TAB for minimal packaging to some extent reduces the concern regarding foreign inclusions in the structure, the point of view of the electrical engineer must also be regarded. The conventional outer packaging of electronic devices performs many vital functions, and discarding it raises a number of issues first considered during the original development of commercial plastic encapsulated integrated circuits in the late 1960's and early 1970's [6]. These may be considered primarily problems of isolation: electrical, chemical, and mechanical.

Most obvious among these concerns is that of electrical insulation from the surroundings. Clearly a TAB device must be protected from the graphite fibers in the surrounding structure which could cause short circuiting; some kind of insulation layer must be provided. Problems may also be raised by the presence of the other component of the composite structure: the resin. Early efforts in the production of plastic encapsulated chips for commercial use were largely centered around solving problems associated with corrosion. Ionic contamination, moisture, and the voltages and currents present in normal circuit operation combined to corrode the metal in the circuit patterns as well as that in the leads. Ionic contamination

can also be a problem for other chip structures as well, since it degrades the quality of the high-purity oxide layers required for the operation of some field effect transistors. Conventional packaging materials were developed that are carefully formulated to avoid the presence of ionic contamination, something which is not true for structural epoxy resins. In addition to providing electrical and chemical isolation, the package must also be thermo-mechanically compatible. At design operating temperatures and under thermal cycling conditions, mechanical stresses must be kept low enough to prevent sudden or fatigue failure of the metal leads, the metal and oxide layers on the chip, and the chip itself. These thermal and mechanical considerations are also of concern during the composite cure, when the assembly will be subjected to high temperatures and pressures.

In addition to these standard concerns, the electronic components of an intelligent structure are within an environment which is meant to perform under mechanical strain from externally applied loads. This raises concerns similar to those of thermomechanical compatibility.

In this study, a technique for embedding devices has been developed which uses a TAB-like process for minimal ply interruption and provides for electrical and chemical isolation. A series of tests was performed to examine the performance of the embedded devices with respect to some of the issues mentioned above, and to explore possible failure modes. A number of devices were embedded in laminates which were formed into structural test coupons; the resulting test articles were subjected to quasi-static and cyclic loads to test the effects of externally applied structural loads on the electronic behavior of the devices and to provoke stress-induced failures of the silicon substrate, metal and oxide layers, or leads. Other test articles were subjected to a high-temperature, high-humidity environment while under electrical bias

(THB) to induce corrosion or other failures associated with moisture and ionic contamination. In the following sections, both the embedding technique and the tests performed on the resulting test articles are described in detail.

3.2 Description of Test Articles and Manufacture

In the work presented here, a number of chips attached to flexible leads by a method similar to TAB were embedded in graphite epoxy laminates, and the resulting parts were cut into mechanical and THB test articles. The embedded device will now be described, followed by details of the manufacture of the test articles.

3.2.1 Selection of the device to be embedded

The first issue addressed was the choice of a TAB packaged chip to use in the investigations. A device with a very simple functionality was sufficient to demonstrate an embedding capability. It was not necessary that the device perform any specific task; a very simple functionality would have the advantage of a sort of transparency, in that its lack of complexity would make it easier to distinguish and understand basic failure modes. Since the difference between very complex and very simple integrated circuits is largely one of scale of integration, and since the failure mechanisms anticipated did not depend on specific device characteristics, it was concluded that a very simple test device would be sufficient to demonstrate the possibility of embedding integrated circuits in general.

As mentioned previously, the technique of tape automated bonding was introduced as a means of simplifying the attachment of leads to chips with large numbers of leads. Discussions with production personnel at a

number of electronics manufacturers soon established that a relatively simple standard component on the level of an op-amp (typically eight leads) or lower was extremely unlikely to be available in TAB form precisely because the low lead count made such a bonding technique unnecessary, whereas the use of a complex device with many leads would complicate analysis of electronic behavior. A specialty device, however, was found which combined a lead attachment process similar to TAB with simple electronic functions.

The device chosen for embedding in this work was the low conductivity integrated circuit dielectric sensor chip manufactured by Micromet Instruments, Inc [5]. This sensor was designed to measure the dielectric properties of epoxy resins during cures for the purposes of polymer research and quality and process control. As it was intended to be embedded in and cured with composite materials, it was well suited to be the test device for this study.

The dielectric sensor chip shown in Figure 3.1 consists of a sensing region with interdigitated electrodes and a circuit region with two NMOS field effect transistors (FETs) and a thermal diode. A schematic diagram of the on-chip circuit elements is presented in Figure 3.2. In normal operation, an excitation in the form of externally generated sinusoidal voltage is applied to one of the electrodes, producing a corresponding voltage on the other electrode, the relative amplitude and phase of which depends on the dielectric and resistive properties of the resin connecting the electrodes. This

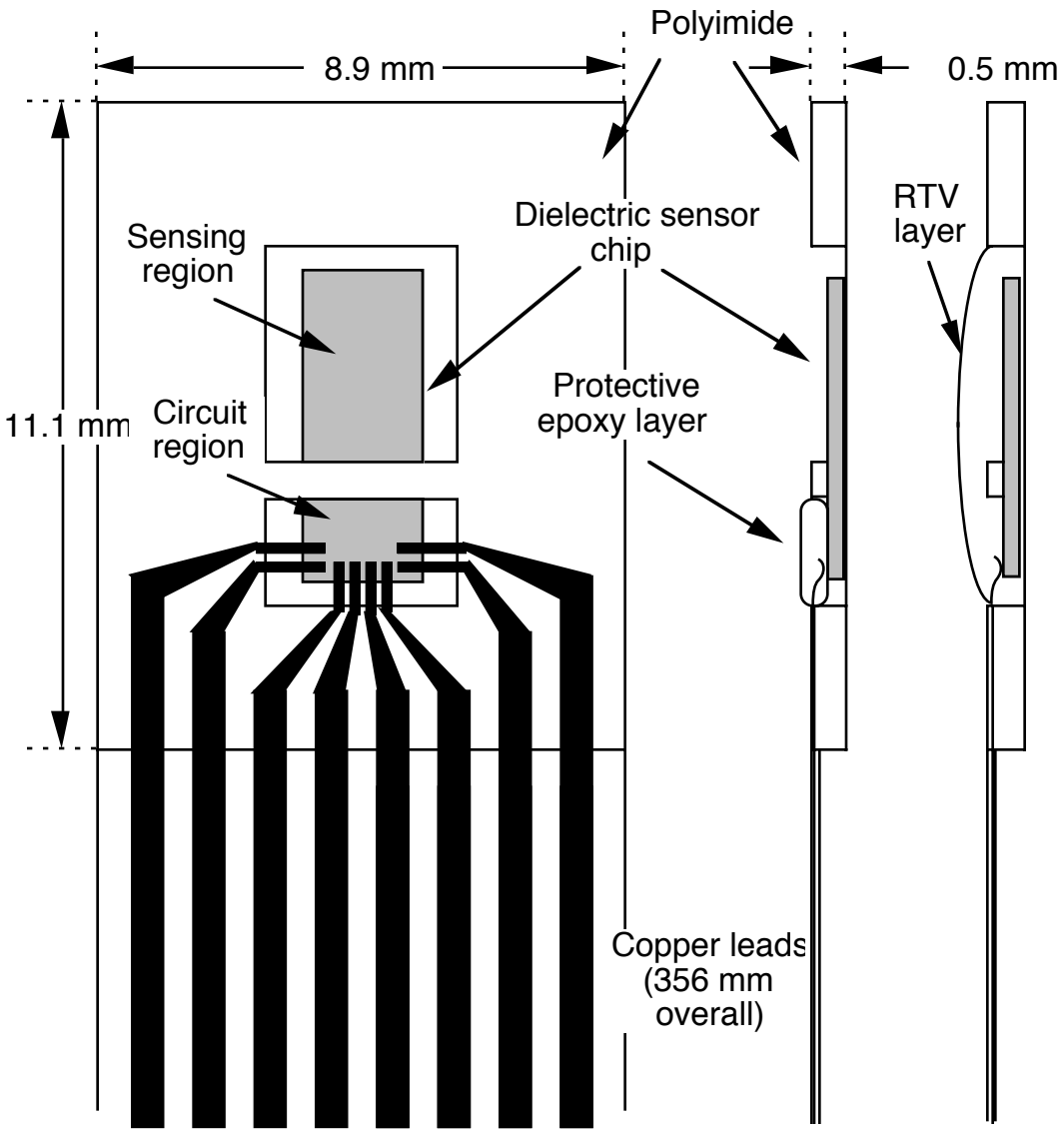


Figure 3.1 **Enlarged view of Micromet dielectric sensor chip and lead attachment. Typical cross-sections show chip with standard protective epoxy layer and with RTV silicone isolation layer.**

receiving electrode is connected to the gate of the signal transistor, modulating the current passing through it. More external circuitry is used to form a feedback loop in which the current through the reference transistor is made to match that of the signal transistor. Since the two FETs are closely matched in their response characteristics and are at the same temperature, the gate voltage on the reference transistor mirrors that on the signal transistor.

This response voltage, buffered and insensitive to external noise, can be used to calculate the resin properties which change as the cure progresses.

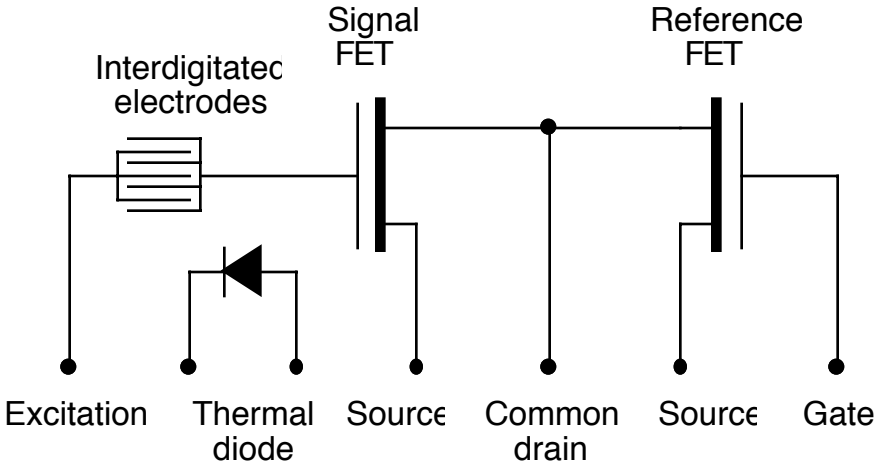


Figure 3.2 **Schematic of the on-chip dielectric sensor components. The p-side of the diode is also the substrate connection. External circuitry is not shown.**

As the structural epoxy dielectric and resistive properties were not the focus of this study, the device was not used as part of the Micromet dielectric measuring system. Instead, the tests described in later sections involved a circuit which measured the characteristics of the reference FET. Connections to the substrate and the source, drain, and gate terminals of this FET were accessible from four of the leads. Another measure of chip and lead integrity was afforded by the monitoring of p-n junction voltage drops. These were measurable across the temperature sensing diode as well as across the junctions formed by the common drain and substrate and the sources and substrate.

Details of the packaging and the leads of the sensor are shown in Figure 3.1. The TAB-like features are apparent, with the patterned copper leads projecting into the window to form the bonds with the chip. The devices used in this work were embedded with two different kinds of material to

provide the necessary electrical, chemical, and mechanical isolation layer, as shown in the cross-sections in the figure. As normally provided by Micromet, the devices have a pre-cured layer of electronics-grade epoxy covering the electronic structures and the copper leads near the bonding points. This standard protective epoxy, type H70E from Epoxy Technology, Inc., protects the fragile copper leads and bonds from damage during handling and provides passivation, protecting the circuit elements from damage due to ionic contamination. It also serves as a barrier against pieces of conductive graphite fiber which might otherwise come into contact with the circuit elements or leads and cause short circuiting. Short circuiting of the electrodes is prevented by the placement of a layer of glass filter paper over the chip which blocks the graphite but is porous to the resin matrix, allowing it to come into contact with the electrodes for dielectric measurements.

It was conjectured that during the loading of the test articles with the standard protective epoxy layer, the epoxy might serve to transfer loads from the structure proper to the leads and chip, leading to breaking or debonding of the leads, or to fracture of the chip itself. A number of devices were therefore prepared in which the epoxy was omitted and the entire upper surface of the chip was covered with a layer of RTV silicone rubber, the idea being that the compliance of the silicone would lead to lower stress concentrations than the rigid epoxy, thus allowing the attainment of greater structural loads before the failure of the device. The RTV silicone chosen was Hipec 3-6550 semiconductor protective coating manufactured by Dow Corning. According to the manufacturers' data sheets, the cured RTV silicone has a Shore A durometer rating of 24 points and a maximum elongation of 400%, while the corresponding values for the epoxy are 88 (Shore D) and 1.72%. Like the epoxy it replaced, the RTV silicone is considered to be electronics-grade; that

is, it is sufficiently free of ionic impurities for use as a passivation layer for integrated circuits. The RTV silicone is sold in the form of a suspension in xylene which was applied to the surface of the chip in two layers and left undisturbed at room temperature for 24 hours. During that time, the xylene evaporated, leaving as a deposit on the chip an RTV silicone layer which had the consistency of a rubbery, resilient gel. The devices treated in this fashion were placed in the composite layup in the same manner as those with the epoxy layer.

The choice of specific ply orientations for the layup of the test articles was made on the basis of the physical dimensions of the device package, and a desire to keep the test matrix simple. Although the dependence of the results of mechanical tests on ply number and orientation would be important to a designer considering the application of this technique, it was decided that a single, very simple layup would suffice for the purposes of this work, since the goal was a feasibility demonstration and the investigation of device failure modes, rather than the establishment of an exhaustive design data base. The thickness of the chip with its surrounding polyimide was 0.48 mm (0.019") and that of the Kapton-encased leads was 0.13 mm (0.005"). Given a nominal ply thickness of 0.135 mm (0.005") for AS4/3501-6, these dimensions can be expressed as roughly four plies and one ply, respectively. This indicated the number of plies which had to be cut to accommodate the embedded device, and led to the adoption of the layup scheme shown in Figure 3.3. The nominal description of the ply layup is $[0°/90°/0°_2]_S$; rectangular holes were cut in three of the interior plies, while the fourth was notched along half its length to accommodate the leads. The outer 0° plies were to provide out-of-plane load transfer past the chip, while the 90° plies were included to provide additional strength in the transverse direction and

make the coupons less subject to damage in handling.

Details of the preparation, layup, and curing of these laminates are given in the next two sections.

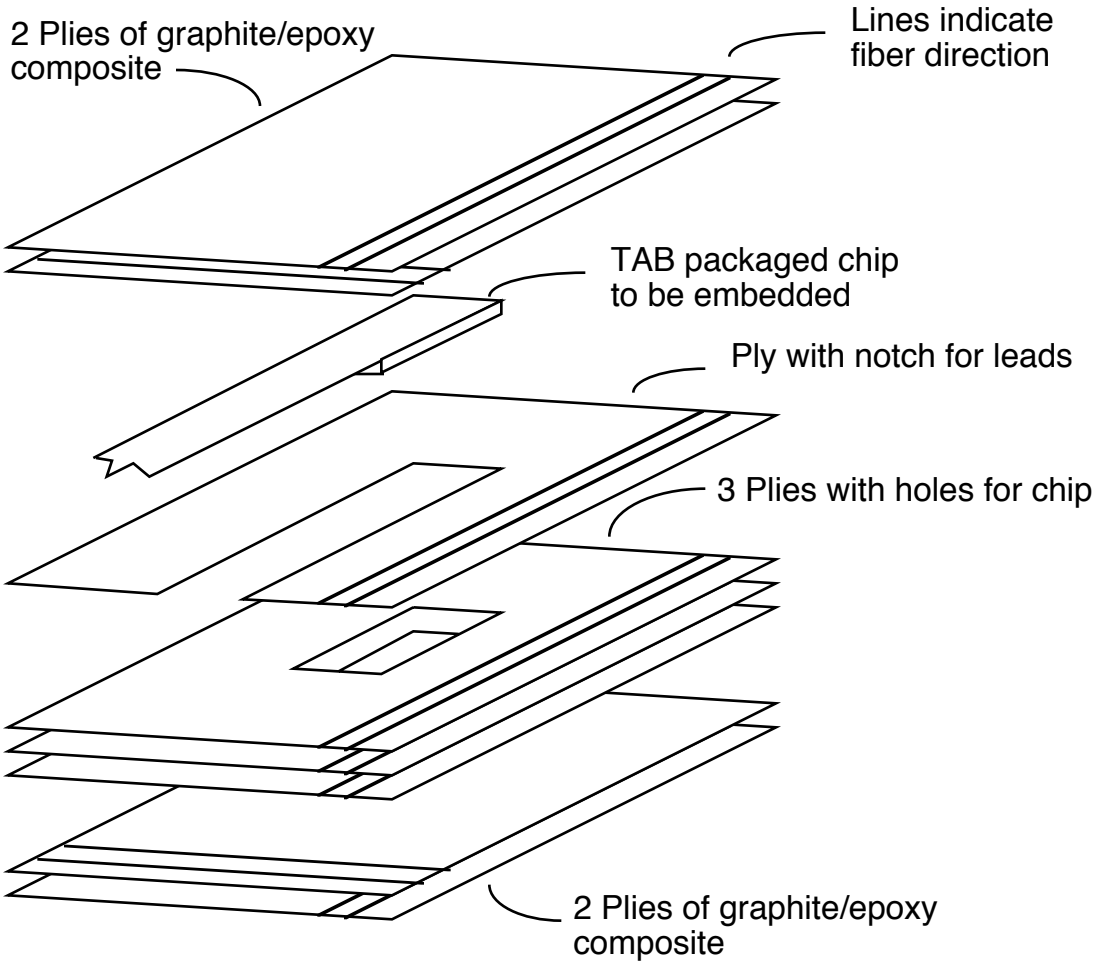


Figure 3.3 **Expanded view of ply layup showing fiber orientation, holes, notch, and device placement.**

3.2.2 Preparation and layup

The test articles used in this work were manufactured according to procedures developed at M.I.T.'s Technology Laboratory for Advanced Composites (TELAC) [26]. These procedures will now be described, as will the details of additions and modifications to them associated with provisions made for embedding the chosen device.

The composite material used was AS4/3501-6 graphite epoxy manufactured by Hercules. It consisted of unidirectional fibers pre-impregnated with resin, B-stage cured, and formed into a 305 mm wide (12" nominal) tape rolled onto a spool with a layer of backing paper . This pre-preg was stored at a constant -18 C (0 F) to maintain its incompletely cured state for long periods. It was allowed to warm up to room temperature for 30-60 minutes after removal from the freezer, which increased the tackiness of the resin and facilitated handling; the layup room was kept at around 24 C (75 F). During the warm-up time the pre-preg was kept in its plastic storage bag with a silica desiccant to prevent moisture condensation. Once removed from the storage bag, it was handled with gloves to prevent contamination from skin oils.

After the pre-preg had warmed to room temperature, it was placed on a spindle and unrolled a few feet at a time for cutting into plies. Each ply was cut to measure 305 mm x 356 mm (12" x 14" nominal) using a utility knife with a razor blade. Rectangular aluminum templates of the correct dimensions were used as guides for cutting. The templates were 3 mm (0.125") thick and were covered with teflon coated glass fabric (TCGF) to prevent adherence of the cut plies to the template. 0° plies were cut in single pieces with the fibers running parallel to the long axis of the ply, but the 90°

plies could not be cut this way, as the roll of pre-preg was too narrow to cut a single piece measuring 356 mm (14") against the fiber direction. Each 90° ply was therefore made of two parts: a square segment of pre-preg measuring 305 mm (12") on a side, and a small strip of the same size in the fiber direction but only 51 mm (2") against the fiber direction. Laid side by side these two segments formed a 90° ply of the desired dimensions with a matrix joint along the line where they met.

Once the desired number and type of plies had been cut, the holes for the cavity into which the chip would be placed (see Figure 3.3) were made. For each laminate, four rectangular holes measuring 9.5 mm by 12.7 mm (0.375" by 0.5") were cut into each of three 0° plies with a utility knife using a TCGF covered piece of cardboard for a template. A similar template was used to cut notches 9.5 mm wide in a fourth 0° ply. The holes and the interior end of the notches were aligned on the transverse axis of the ply and spaced 75 mm (3") apart so that each laminate could accommodate four embedded devices. For the laminates intended for use as THB test articles, the holes and notches were placed closer to the edge but with the same transverse spacing. The templates used for cutting the plies are shown in Figure 3.4.

After the holes and notches had been cut in the interior plies, the laminates were assembled. This was performed on a jig consisting of a flat table covered with double-sided tape and with two aluminum guide bars running along two sides and forming a right angle at one corner of the table. The first, bottom-most 0° ply was placed in the jig with the backing paper down on the sticky surface. Subsequent plies were similarly placed but with the backing paper facing up, the metal guides serving as aids to align the plies in translation and rotation. After each ply after the first was placed and pressed down and smoothed by hand, the backing paper was peeled off,

exposing the surface for the placing of the next ply.

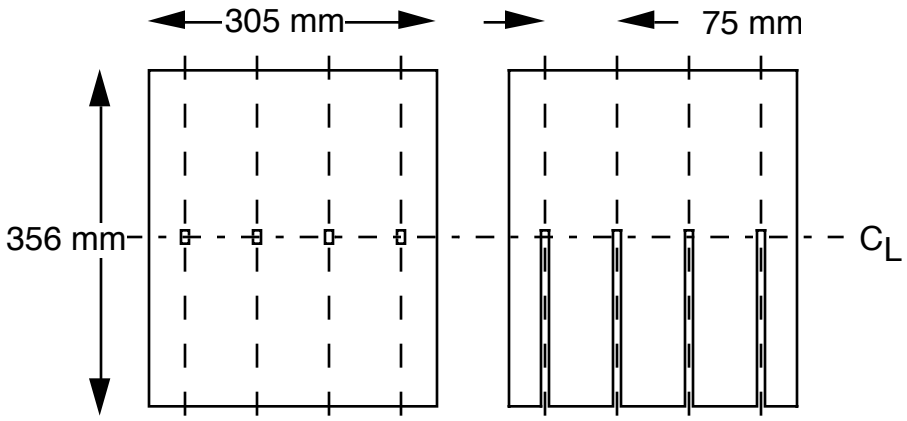


Figure 3.4 **Teflon covered cardboard templates used for cutting holes and notches in pre-preg plies to accommodate four chips and their leads in one laminate.**

This procedure was followed in placing the outer 0° ply, the neighboring 90° ply, the three interior 0° plies with holes and the 0° ply with notches. At this point, a device was placed in each of the four cavities formed by the holes in the assembled plies, and the leads were aligned to lie in the notches. The chips were seated in their cavities by pressing gently on the surrounding polyimide to avoid damaging the lead connections to the chip. A piece of 0.28 mm (0.011") thick #34 glass filter paper (manufactured by Schleicher & Schuell) measuring approximately 3.2 mm by 6.4 mm (0.125" by 0.25") was placed over the silicon chip. The purpose of this paper was to provide a semi-permeable layer over the interdigitated electrode area on the chip; the glass filter allowed the resin to flow onto the electrodes during the cure so that the dielectric properties could be monitored, while at the same time keeping away graphite fibers and particles which could short the electrodes. Although only a few of the devices described were monitored during the cure in this way, the filter was included in all test articles to avoid

introducing undesirable variations. While the glass paper was probably not needed to prevent shorting of the active electrical components on the devices with the fairly hard standard protective epoxy layer, it may well have served this function for the chips covered with the much softer silicone isolation layer. In either case, the porosity of the glass would not have presented a barrier to moisture or ionic contaminants.

After placement of the devices and the glass filter paper, the remaining 90° and 0° plies were laid on top of the assembly to complete the layup. The resulting laminate was then removed from the jig and the remaining pieces of backing paper were peeled off and replaced by sheets of peel-ply. The peel-ply layers, permeable nylon sheets manufactured by Burlington Impression Fabrics, provided a textured finish to the surface of the cured part. Excess graphite/epoxy and peel-ply were trimmed from the three sides of the laminate, which was then ready for curing.

3.2.3 Cure assembly

The assembled laminates were cured on an aluminum caul plate. The caul plate was prepared by coating it with the mold release agent Mold-Wiz and covering it with a sheet of non-porous teflon coated glass fabric (TCGF). A T-shaped aluminum dam and an aluminum top plate was positioned on the caul plate, and strips of adhesive backed corprene rubber (type DK-153T manufactured by I. G. Marston) were used to hold the aluminum dam in place and to form the other two sides of the rectangular well in which the laminate is to be placed, as shown in Figure 3.5. The T-dam and top plates were removed, and the T-dam was sprayed with the mold release agent Frekote and replaced on the caul plate.

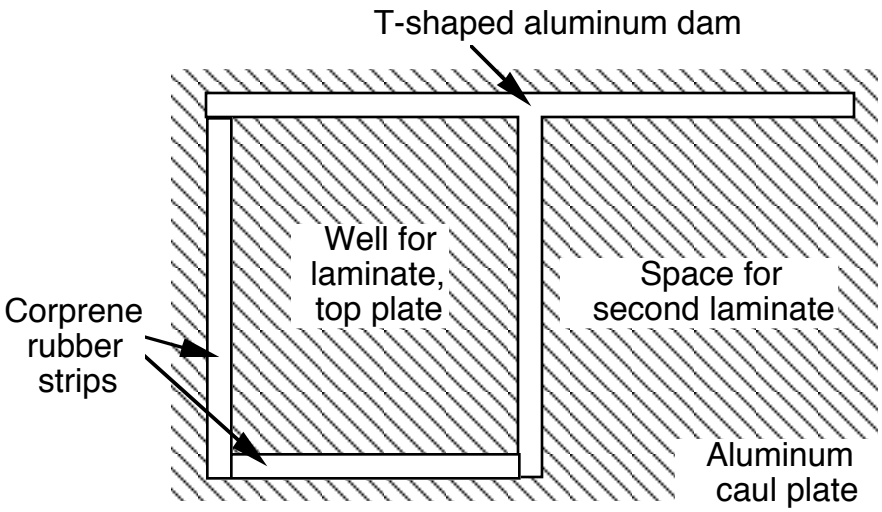
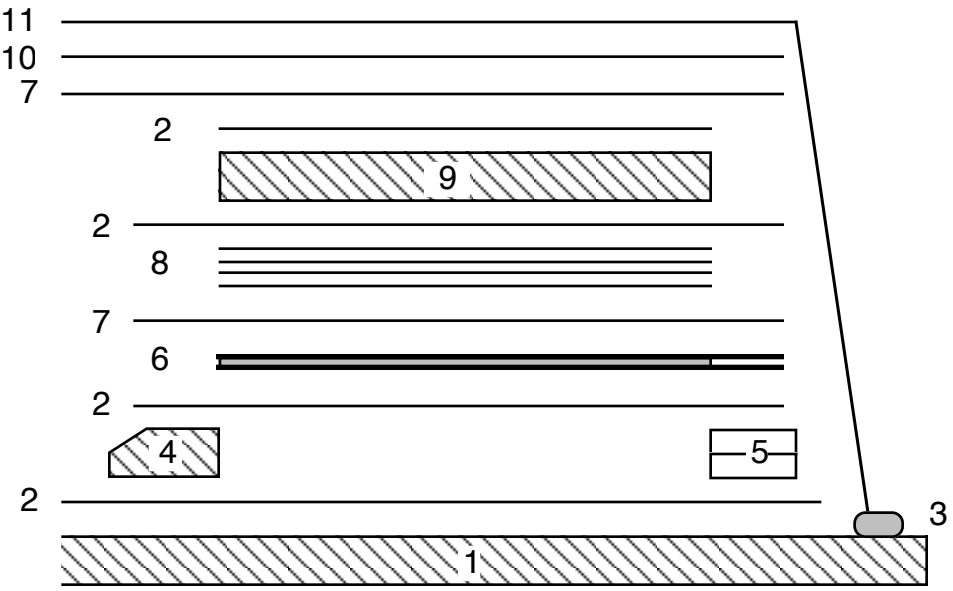


Figure 3.5 **Layout of T-dam and corprene rubber strips on aluminum caul plate to form well for composite laminate.**

A diagram illustrating the various components of the cure assembly is presented in Figure 3.6a. A sheet of non-porous TCGF 25 mm (1") larger than the laminate on each side was placed in the well and the laminate was placed on top. At this point allowance had to be made for the leads projecting from one side of the laminate, as shown in Figure 3.6b. Although the excess fringe of the peel-ply and non-porous TCGF normally lie on top of the dam, it was necessary to keep the leads relatively flat to avoid crimping them between the dam and top plate. Small slits were therefore cut in the peel-ply and underlying TCGF sheet; the leads ran through these slits and under the corprene rubber dam, which was temporarily lifted up to allow this. In order to prevent the corprene rubber dam from adhering to the leads after the cure, small sleeves of non-porous TCGF were wrapped around the leads.



Key:
1. Aluminum Caul Plate
2. Non-porous Teflon Coated Glass Fabric
3. Vacuum Tape
4. Aluminum Dam
5. Corprene Rubber Dam
6. Laminate Covered with Peel Ply
7. Porous Teflon Coated Glass Fabric
8. Paper Bleeder
9. Aluminum Top Plate
10. Glass Cloth Air Breather
11. Vacuum Bag

Figure 3.6a **Schematic cross-section of the cure assembly.**

The laminate was then covered by an oversize piece of porous TCGF, followed by four layers of paper bleeder (one for every two plies in the laminate) to soak up excess resin. Another oversize sheet of TCGF was laid on top of the bleeder followed by the top plates, which had been coated with Frekote, and another sheet of TCGF. The entire plate was then covered with pieces of porous TCGF, followed by a sheet of glass breather cloth. This provided the air passages necessary for the even application of vacuum to the assembly. Finally, a bead of vacuum tape was applied along the exposed

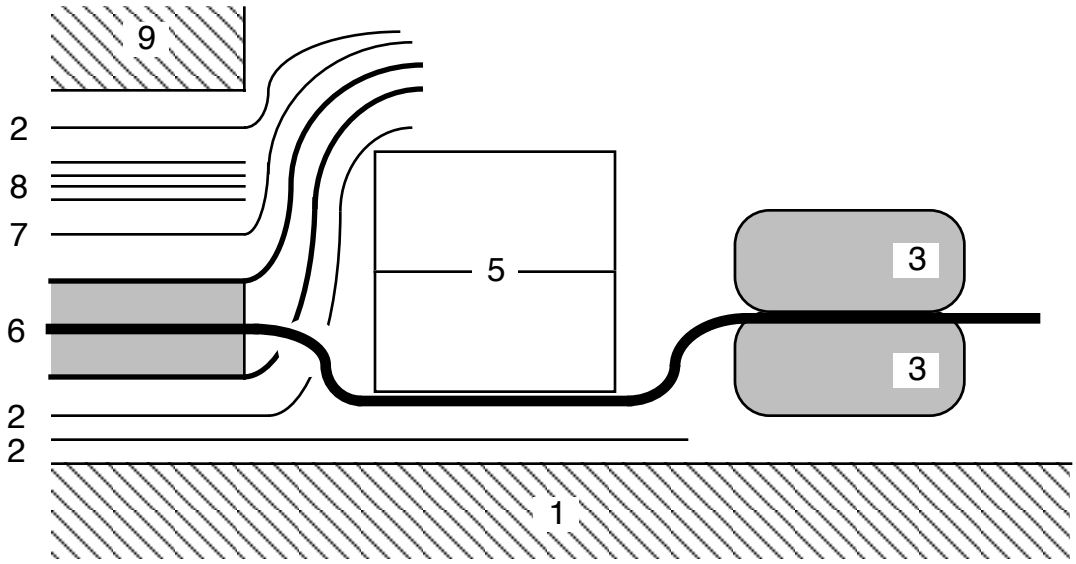


Figure 3.6b **Detail of routing of leads around corprene rubber dam and through vacuum tape seal. Legend is that of 3.4a. Note that device leads (heavy line) pass through slits, under corprene rubber dam, and between vacuum tape layers.**

outside edge of the caul plate and a piece of vacuum bag was placed over the entire assembly, producing an airtight enclosure open only at the attachment to the vacuum ports. In order to allow the monitoring of the devices during the cure, the leads were brought out of the vacuum enclosure by routing them over the bead of vacuum tape and covering them with a second bead of tape for the seal to the vacuum bag.

3.2.4 Cure schedule and yields

After the cure assembly was complete, the air within it was evacuated using a mechanical pump. The vacuum seal was considered sufficiently good when a vacuum was maintained to within 1" Hg of 29" Hg over five minutes with the pump shut off. Following successful completion of this test outside the autoclave, it was repeated inside the autoclave. Then the vacuum was turned on again and the autoclave was pressurized to 0.59 MPa (85 psig).

Upon reaching the desired pressure, the heaters were turned on and the cure cycle began. The vacuum, pressure, and temperature profiles during the cure are shown in Figure 3.7.

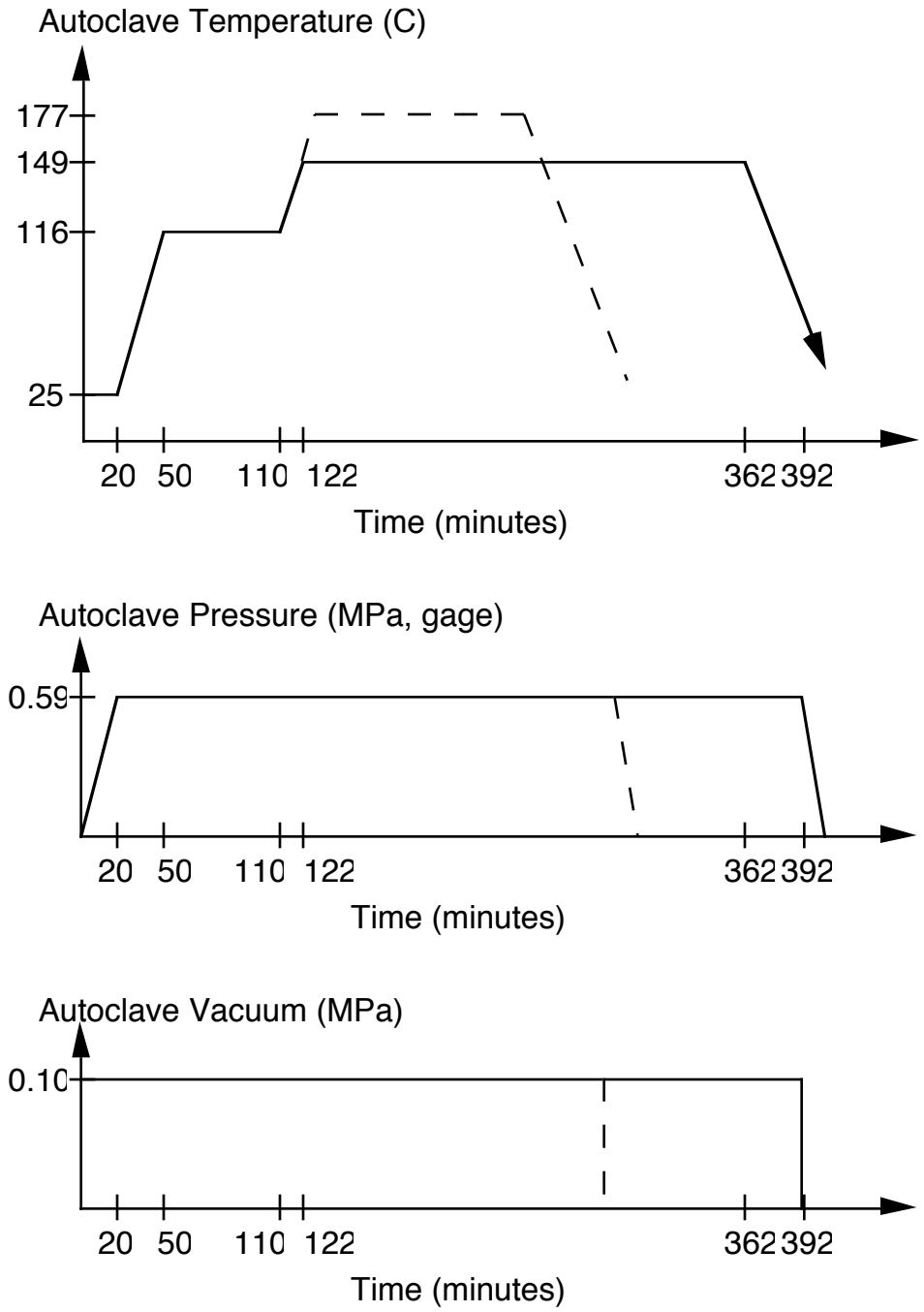


Figure 3.7 **Temperature, pressure, and vacuum histories during the AS4/3501-6 graphite/epoxy cure; dashed line is the standard cure, solid is the modified scheduled followed in this work.**

The two temperature stages perform two functions. During the one hour hold at 116 C (240 F), the viscosity of the resin decreases and it starts to flow, allowing the plies to merge and settle under the pressure. The high temperature stage at 149 C (300 F) drives the epoxy cross-linking reaction to near completion. The heating is performed by forced air convection past electric heating coils, and the cooling is effected by passing the air over tubes containing chilled water. Both the heating and cooling rates are kept to roughly 3 C/minute (5 F/minute), the latter to prevent the occurrence of thermal shock.

It should be noted that the standard cure cycle calls for a high temperature stage of two hours at 177 C (350 F) as opposed the four hours at 149 C (300 F) used in the cures in this work. The conventional profile was used on the first three trial cures involving ten devices, but six of these devices were found to fail during the cure, giving a yield of only 40%. Those failed devices which were monitored during the cure by the Micromet instrument showed erratic data starting at some point in the high temperature stage, and measurements of diode drops across some of the leads with a Fluke 77 multimeter were off scale, indicating open circuits. Since the resin should have already settled during the low temperature cure stage, and the temperature was not changing at the time of failure, the phenomenon could not be explained by mechanical loads induced by mismatch of coefficients of thermal expansion.

On the hypothesis that the failures might be due to some abrupt change in the specific volume upon passing through the glassification temperature, the longer and cooler cycle was tried. Five cures were performed using this modified schedule. Four of these involved 26 devices with the standard protective epoxy, of which 15 survived for a yield of 58%, and one cure

involved eight devices with the RTV silicone isolation layer, of which three survived for a yield of 38%.

A final deviation from the standard cure was the omission of an 8 hour post cure at 177 C (350 F) and atmospheric pressure. This post cure is meant to drive the epoxy reaction still further, producing some increase in fracture toughness but little change in elastic properties. Since this operation is generally not performed in industry, and to avoid the possibility of still further decreases in yields of functional devices, the post cure was eliminated.

Type of Test Article	Type of Test		
	Static Mechanical	Cyclic Mechanical	Temperature/ Humidity/Bias
With epoxy layer	E-STAT-1	E-CYC-1	THB-1
	E-STAT-2	E-CYC-2	THB-2
	E-STAT-3	E-CYC-3	THB-3
With RTV layer	R-STAT-1 R-STAT-2	R-CYC-1	-
Standard cure, non-functioning device	NFD-STAT-1 NFD-STAT-2	-	-
Standard cure, no device	ND-STAT-1 ND-STAT-2	-	-

Table 3.1 List of test articles, ordered by characteristics and type of test.

Table 3.1 presents an overview of all the test articles used in this investigation and their code designations. Note the inclusion of the four test articles with non-functioning devices or no devices. These are from the preliminary trial cures performed with the standard cure schedule, and were included in the static mechanical tests to provide some indication of the separate effects that the inclusion of a device and the modified cure might

have on the modulus and strength of the coupon.

3.2.5 Machining, loading tabs, and instrumentation

The cured laminates were machined into coupons of the appropriate sizes using a milling machine fitted with a diamond abrasive disk and a water jet for cooling and dust removal. The disk rotated at the spindle rate of 1100 RPM, and the table to which the laminates were clamped was translated under the disk at 200 mm (8") per second. Two kinds of test articles were machined in this way: those intended for mechanical testing, and those intended for THB testing.

The mechanical test articles were machined to standard TELAC coupon dimensions, shown in Figure 3.8. The coupons measured a nominal 356 mm (14") in length and 50 mm (2") in width. The coupons were milled so that the device chips were centered both longitudinally and transversely, and the leads ran half the length of the coupon to emerge at one end. The thickness of the coupons measured at locations away from the chip varied from 1.04 mm to 1.12 mm (0.041 to 0.044"). The coupons containing the devices with the standard protective epoxy layer measured 1.14 to 1.17 mm (0.045 to 0.046") in thickness at the chip location, while the coupons with RTV silicone isolated devices measured 1.24 mm (0.049"). Since the slight excess resin on the surfaces tends to give slightly oversized thickness measurements, especially for thin laminates, while contributing little to the strength or stiffness, a nominal thickness of 1.07 mm (0.042") was assumed for later stress calculations.

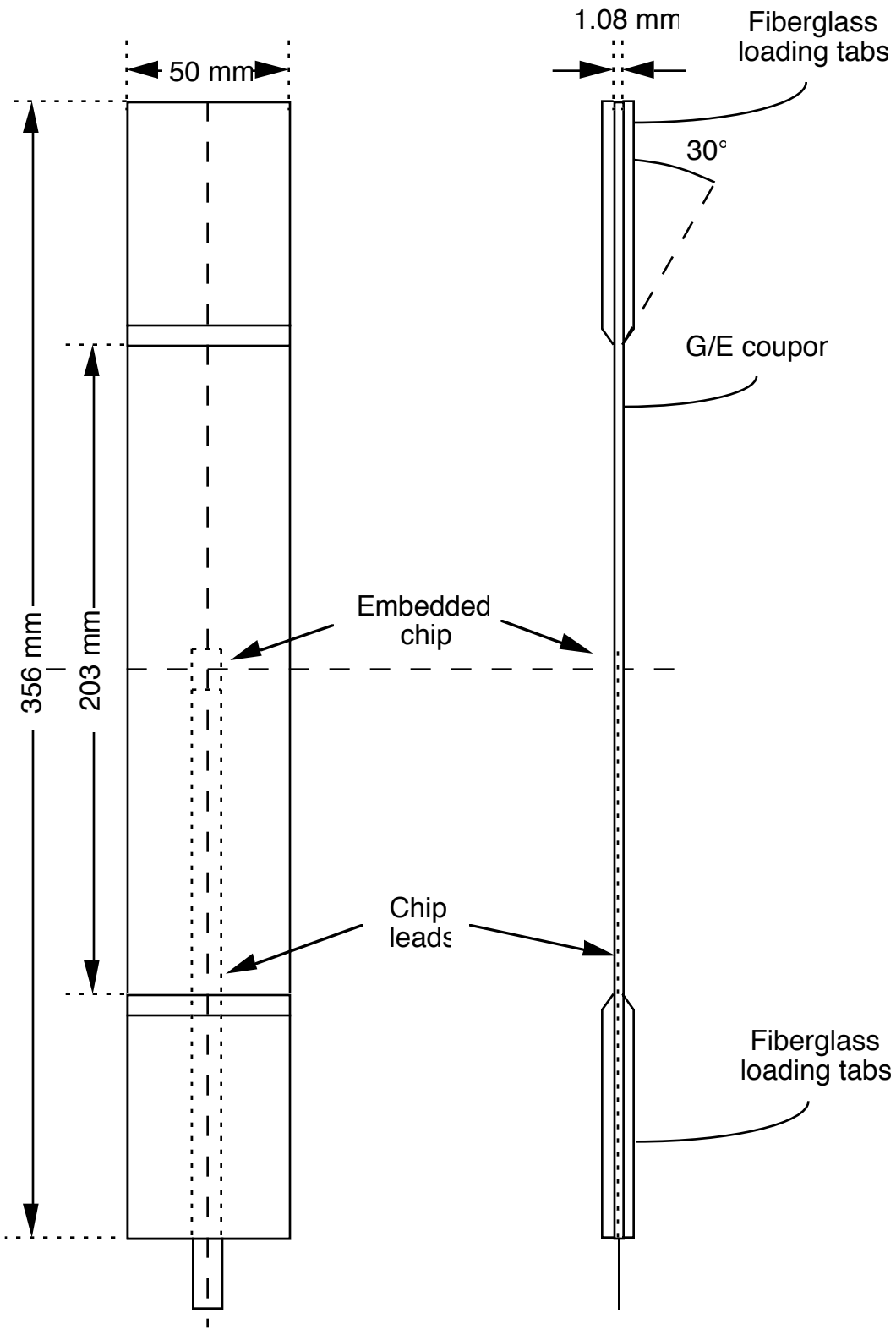


Figure 3.8 **Test article for static and cyclic mechanical tests.**

In order to apply uniform loads to the mechanical test articles, loading tabs were required to prevent the testing machine grips from producing local stress concentrations and damaging fibers near the surface. The loading tabs were manufactured from stock sheets of 11-ply laminates of 3M Scotchply SP-1002 pre-cured glass/epoxy with a nominal thickness of 2.8 mm (0.11 in). The fiberglass was milled into 50 mm (2") strips to match the width of the coupons, and the strips were then cut into 75 mm (3") lengths on a bandsaw. A 30° bevel was then put on one end of the resulting pieces by means of a belt sander. After the loading tabs were abraded with sand paper to provide a roughened surface, they were bonded to the ends of the coupons using Epoxi-patch 0151-Clear, a two-part room-temperature curing epoxy manufactured by Dexter Corp., Hysol Division. The coupons with loading tabs were placed on a flat surface and loaded with 4-5 kg (9-11 lb) of lead weights to hold the tabs in place, squeeze out the excess epoxy, and produce a uniformly thing bonding layer. This overnight room temperature cure deviates from standard TELAC practice; normally FM-123-2 film adhesive manufactured by American Cyanimid is used which is cured for two hours at 107 C (225 F) with a vacuum and an applied pressure of 0.068 MPa (10 psig). The alternate loading tab bonding scheme was used to avoid the possibility of undesired device failures due to further temperature cycling.

Some of the mechanical test articles thus prepared were then instrumented with strain gages. The gages used were EA-06-125-AD precision foil gages manufactured by Measurements Group, Inc. These had a gage factor of 2.055±0.5% and consisted of a 120±0.15% ohm, 3.175 mm (0.125") square constantan wire element on a 0.025 mm (0.001") thick polyimide substrate. They were bonded to the coupons in four places as shown in Figure 3.9. The longitudinal and transverse gages far from the center were intended to yield a

far-field check on the elastic properties of the composite material, while the two longitudinal gages at the mid-length station of the coupon provided a measure of the strain concentrations produced by the inclusion of the chip. Only the test articles intended for static extension testing were equipped with strain gages; those to be used in cyclic mechanical tests were not.

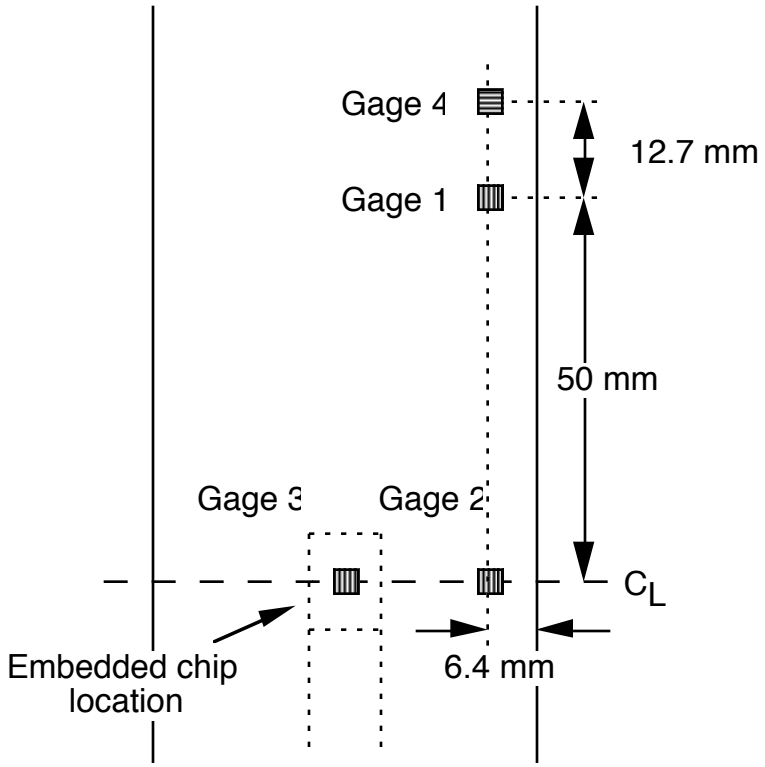


Figure 3.9 **Location of strain gages on coupons for static extension load tests. Lines indicate that gages 1, 2, and 3 are longitudinal, while gage 4 is transverse.**

The test articles intended for the THB test were smaller, measuring 60 mm by 75 mm (2.375" by 3") as shown in Figure 3.10. Unlike the case of the mechanical tests, there was no standard size to follow, so the dimensions chosen were fairly arbitrary. The need for a substantial lead length to allow the use of the intended test oven dictated the nearness of the chips to the edge of the laminate, and the same template spacing was used for cutting the ply

holes and notches as in the laminates intended for use as mechanical test articles. Since the ratio of length or width to thickness was then approximately 55-70:1, it could be argued that performance degradation due to bulk diffusion of moisture and ionic contaminants would be dominated by travel through the thickness of the test article rather than in the plane. This argument however does not address the possibility of preferential moisture migration along the interface between the leads and the composite.

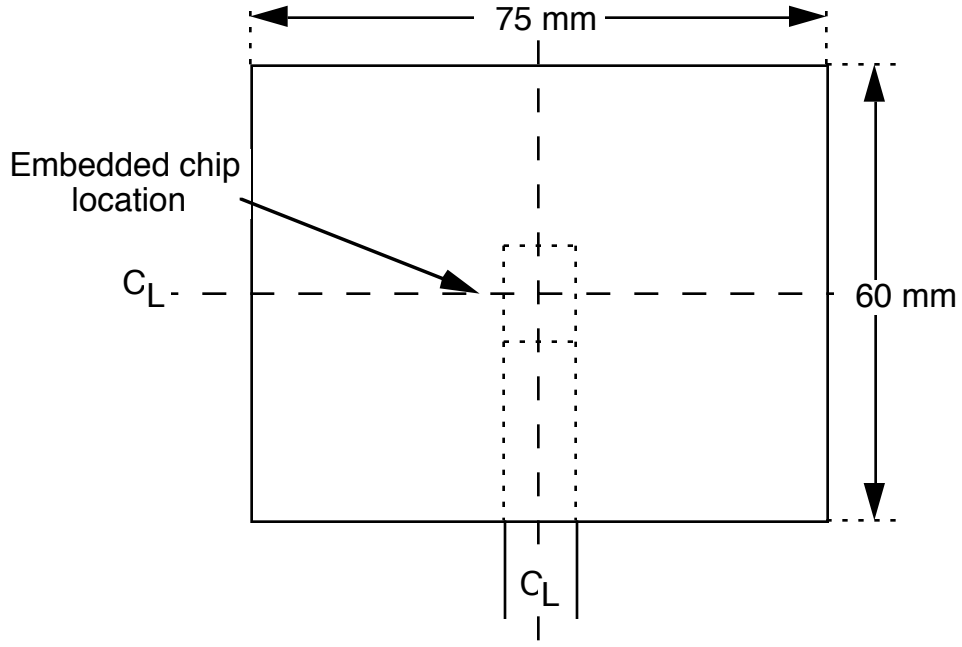


Figure 3.10 **Nominal dimensions of THB test article.**

All the THB test articles prepared had embedded devices with the standard protective epoxy layer rather than the RTV silicone layer. Although the RTV silicone also provided passivation, it was primarily chosen as a compliant mechanical isolation layer for comparison with the more rigid epoxy. The performance of the RTV silicone with respect to protection against moisture and ionic contamination is relevant, but in this work additional THB tests on devices embedded with the RTV silicone layer were

omitted due to time constraints.

During both mechanical and THB tests the condition of the device was monitored by measuring the function of one of the MOSFETs on the chip. The circuit used for this purpose is shown in Figure 3.11. A constant 10 mV drain-source voltage (VDS) is applied to the device under test and the resulting drain-source current (I_{DS}) is passed through the 1 KΩ feedback resistor to produce a voltage proportional to I_{DS}. When a triangle waveform (approximately 10 V p-p, 10 Hz) is applied to the gate (V_{GS}), I_{DS} varies in a characteristic fashion demonstrating the transistor action. A typical plot of I_{DS} against V_{GS} is shown in Figure 3.12. This curve clearly shows the cut-off V_{GS} and the small-signal transconductance, both of which may be measured and used as quantitative indications of the condition of the transistor, though the nature of the curve changes observed in tests made this unnecessary.

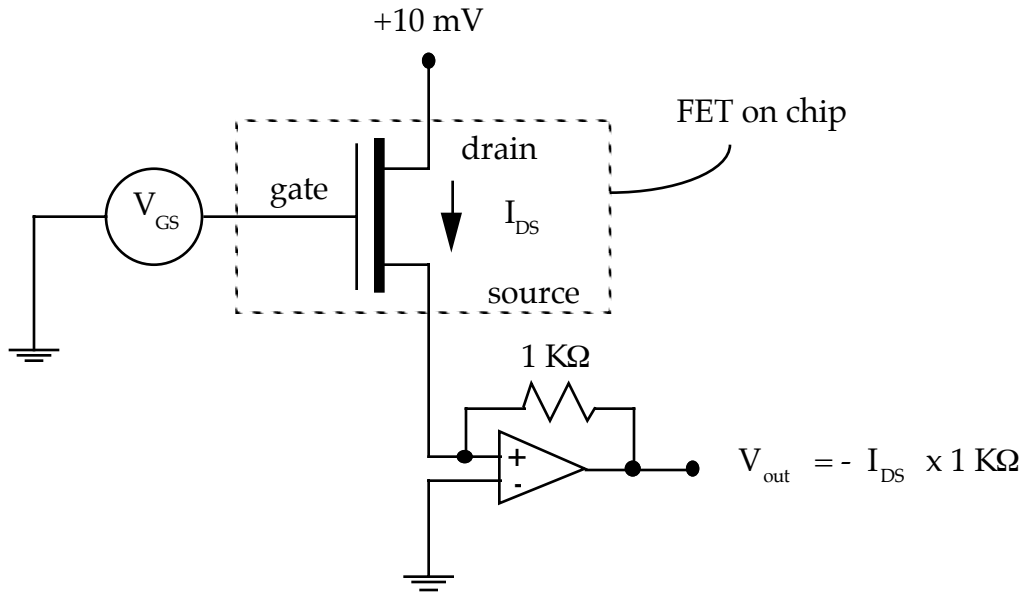


Figure 3.11 **Schematic of circuit to test FET on embedded device (inside dotted line). V_{GS} may be a triangle wave for curve tracing or a constant voltage for monitoring I_{DS} at a fixed operating point with a strip chart recorder.**

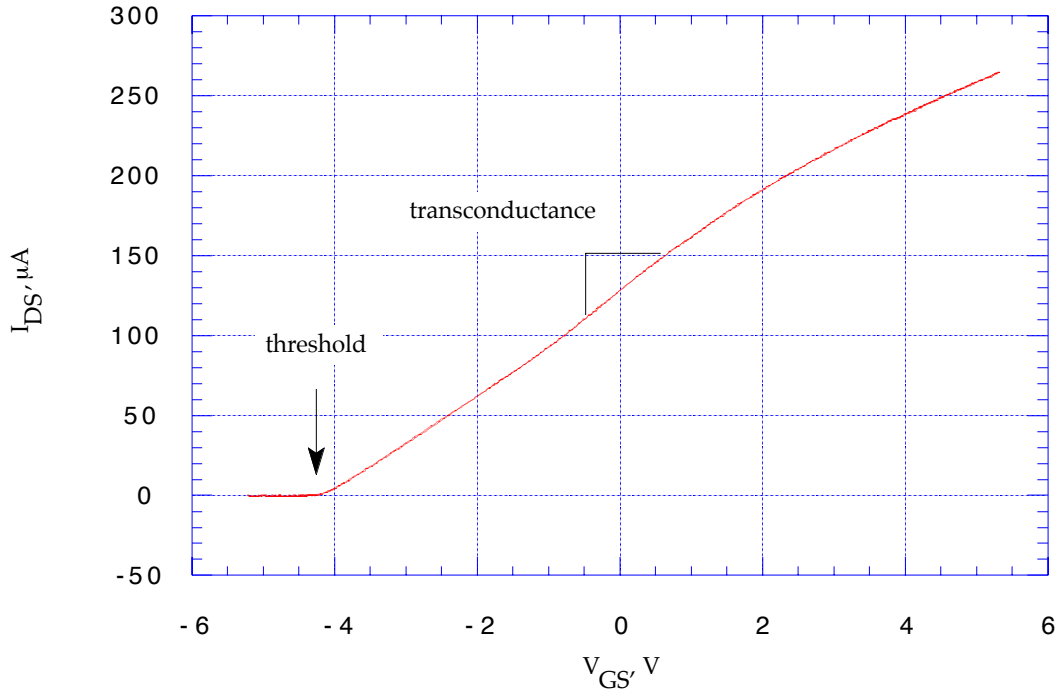


Figure 3.12 **Typical transistor characteristic curve of drain-source current as a function of gate-source voltage shows threshold voltage and small-signal transconductance. Drain-source voltage was fixed at 10 mV. This curve was taken on test article THB-3 at 80 C at the start of the test.**

Transistor curves obtained with this test circuit were stored on disks using a Nicolet digital oscilloscope, but this could only provide an approximately instantaneous picture of the state of the device's electronic behavior. In order to produce a continuous history of circuit behavior for tests expected to run for long periods of time, provisions were made to replace the V_{GS} triangle waveform with a constant voltage. This would produce a test circuit output voltage proportional to the nominally constant I_{DS}. Variations in the transistor behavior would then be reflected by changes in this voltage, which could be continuously plotted for up to four devices using a four-channel Gould Brush 2400 strip chart recorder with DC amplifiers. These continuous measurements could be interrupted from time to time to

capture complete transistor curve traces using the triangle waveform.

In the next two sections, details are given of tests performed on the test articles whose preparation and manufacture has just been described. The performance of the embedded devices under static and cyclic mechanical loading, with both the standard protective epoxy and RTV silicone layers, is investigated, followed by testing of susceptibility to damage induced by heat and moisture in the THB experiment.

3.3 Mechanical Load Tests

Once the capability to produce composite parts with functioning embedded electronic components has been demonstrated, the application of such structures as load bearing members immediately raises questions about the sensitivity of the electronic behavior to applied loads. The basic concern regarding the function of the embedded devices while the structure is under load was tested by subjecting the mechanical test articles to an increasing quasi-static extensional load. The possibility of fatigue failure were explored by the application of cyclic tension-tension loads. Both of these tests were expected to indicate failure modes possibly involving lead fracture, lead debonding, or chip fracture. These tests were further designed to show whether the transistor function would exhibit an undesirable sensitivity to strain at any level.

3.3.1 Procedure description

Static extension tests were performed on a total of five test articles with embedded devices: three with the standard protective epoxy and two with the RTV silicone isolation layer. Each test article was placed in a MTS 810 Material Test System hydraulic testing machine, and the top and bottom grips

were pressurized to 7 MPa (1000 psi). Each of the four strain gages was connected to a Vishay 2120 strain gage signal conditioner attached to a DEC PDP 11/34 equipped with A/D converters and running TELAC automatic data acquisition software. In addition to the strain gage readings, the computer recorded stroke and load from the actuator and load cell of the MTS machine. The leads of the embedded device were connected to the transistor test circuit and the trace of I_{DS} against V_{GS} was monitored on a Nicolet digital oscilloscope.

After the strain gage amplifiers were balanced and the gripping pressure was applied, the hydraulic actuator began to apply the extensional load. The MTS controller was run under stroke control and was programmed to move the actuator head in a ramp profile to produce an elongation of 12.7 mm (0.5") over a period of 1000 seconds. The computer recorded load, stroke, and the four strain readings once every 0.5 seconds for the duration of the test. Transistor curve traces were recorded on magnetic disk before and after gripping. During the loading, traces were recorded every 15 seconds through the first 90 seconds and every 30 seconds thereafter. Additional traces were recorded at unscheduled times when noticeable changes occurred in the transistor curve. At each recording of the transistor curve a mark was placed in the data recorded by the computer so that both scheduled and unscheduled traces could be correlated with the concurrent applied load and strain gage readings.

During the first round of tests of the test articles with the standard epoxy layer, the MTS machine was allowed to continue until gross damage to the laminate was visible and the load level dropped substantially, at which point the controller and data acquisition system were halted. This was done to establish the ultimate strength of the coupons for comparison with the

loads at which the embedded devices failed. As this resulted in the complete fragmentation of the silicon chips and the destruction of their delicate lead connections, subsequent examination of the test articles could yield no additional information regarding the failure mechanism of the devices. To allow such analysis, an attempt was made to stop the tests of the test articles with the RTV silicone layer prior to the complete breaking of the coupons. These tests were stopped shortly after cessation of device function.

Cyclic extension tests were performed on a total of four test articles with embedded devices: three with the standard protective epoxy and one with the RTV silicone isolation layer. Each test article was placed in a MTS 810 Material Test System hydraulic testing machine, and the top and bottom grips were pressurized to 7 MPa (1000 psi). The leads of the embedded device were connected to the transistor test circuit and the trace of I_{DS} against V_{GS} was monitored on a Nicolet digital oscilloscope.

As is usual in fatigue tests and in contrast to the procedure followed in the static tests, the computer data acquisition system was not used to record stroke, load, or strain. Since a large number of cycles (perhaps hundreds of thousands) were originally expected to be completed, data from such measurements would have been so repetitious as to have been meaningless. Instead, a procedure more like that employed in the corrosion test was planned. Since fatigue phenomena generally tend to follow patterns based on the log of the number of cycles (as suggested by the semi-logarithmic scales used in standard S/N diagrams) it was decided to record transistor curve traces on a roughly logarithmic scale, after the first cycle, the third cycle, the tenth cycle, the thirtieth cycle, and so on. During long periods of cycling the behavior of the circuits would be monitored by recording the I_{DS} measurement on the strip chart recorder while under constant V_{GS} bias.

The mechanical loading was in the form of a tension-tension haversine. The test article, once fixed in the grips, was pre-loaded to a tension corresponding to 1/10 of the maximum to be applied, and the MTS controller was then programmed to apply a sinusoidal tensile load varying between this starting level and the maximum. The maximum load was originally chosen to correspond to a nominal tensile stress of 540 MPa (77 ksi) based load levels associated with device failures observed in the static tensile tests. This level and the corresponding 10% minimum load was lowered on some of the later cyclic tests to 410 and 41 MPa (60 and 6 ksi), respectively, in an attempt to obtain more cycles before failure. In each test, the first cycle was performed at 0.01 Hz, the next nine at 0.1 Hz, and all subsequent cycles at 1.0 Hz.

3.3.2 Results

In this section, the results of first the static and then the cyclic mechanical tests will be presented. The effectiveness of the RTV silicone layer in increasing the attainable loads and number of cycles is demonstrated. In addition, the effect of the presence of the chip and leads on the strength and stiffness of the coupons is indicated. An explanation of the device failure mechanism is given, as are the loads and numbers of cycles at which these failures occur.

One of the major objectives of these tests was to observe the behavior of the embedded device when placed under mechanical stress. In all cases, the transistor characteristic curves observed and recorded on the digital oscilloscope showed no dependence on load levels, such as might be due to lead resistance changes with elongation or other gradual effects. The devices themselves did not act as strain gages, and appeared to be insensitive to the load applied to the coupon until device failure. The appearance and nature of

the failure behavior is described below in some detail following the cyclic test results; generally speaking, it manifested itself in both the static and cyclic tests as a sudden replacement of the characteristic curve (like that in Figure 3.12) with a horizontal flat line at or close to zero.

The plots in Figure 3.13 show the load levels at which the embedded devices failed in test articles E-STAT-1, 2, and 3, all of which incorporated devices with the standard protective epoxy layer. The device in E-STAT-1 performed properly up to 7700 μstrain and 750 MPa, which are 57% and 71% of the maximum values of 13500 μstrain and 1050 MPa. E-STAT-2 functioned up to 9000 μstrain and 1010 MPa, 64% and 83% of the maximum values of 14000 μstrain and 1220 MPa, while E-STAT-3 survived only until 2300 μstrain and 260 MPa, 16% and 22% of the maximum values of 14200 μstrain and 1180 MPa.

In each case, cracking sounds were heard around 250 MPa (2400 μstrain), possibly indicating matrix failure. Visible laminate damage first appeared near maximum load in the form of fiber breakage in the outer 0° plies at the chip location, and concluded with the complete fracture of the coupon along the transverse centerline. At the end of such a test, the coupons were damaged to such an extent that the embedded chips were visible and appeared to be shattered. Further tests to determine the exact mode of device failure were therefore impossible.

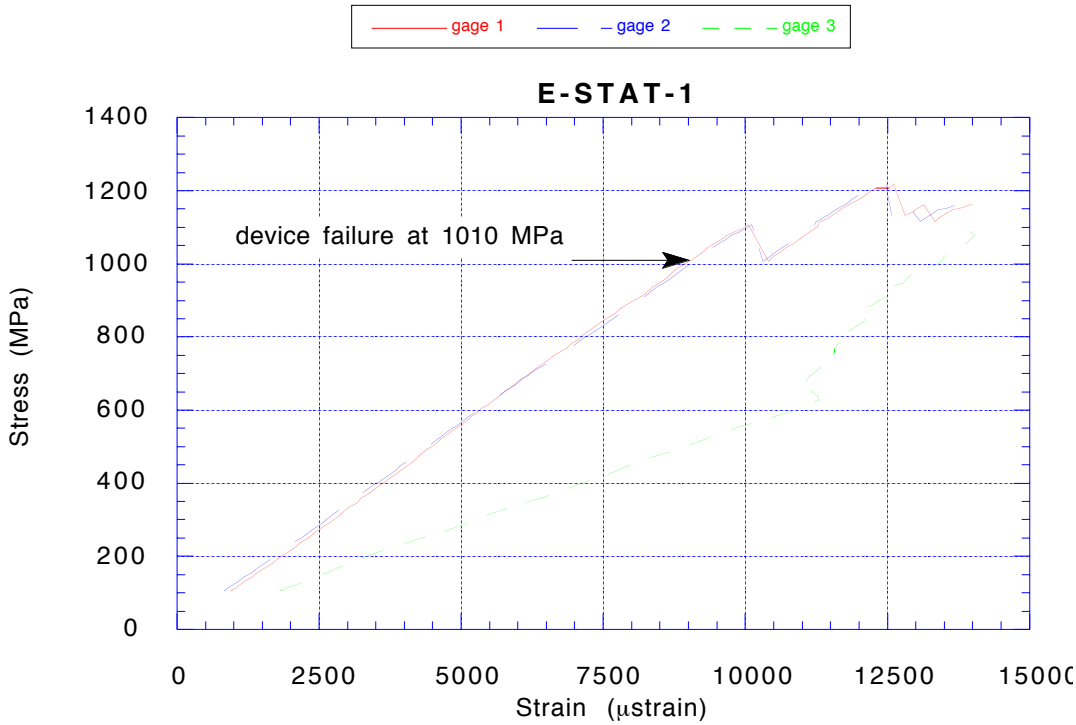


Figure 3.13a **Stress-strain curves of static tension test article E-STAT-1. Longitudinal strain at three locations is shown along with the load level at which transistor function ceased.**

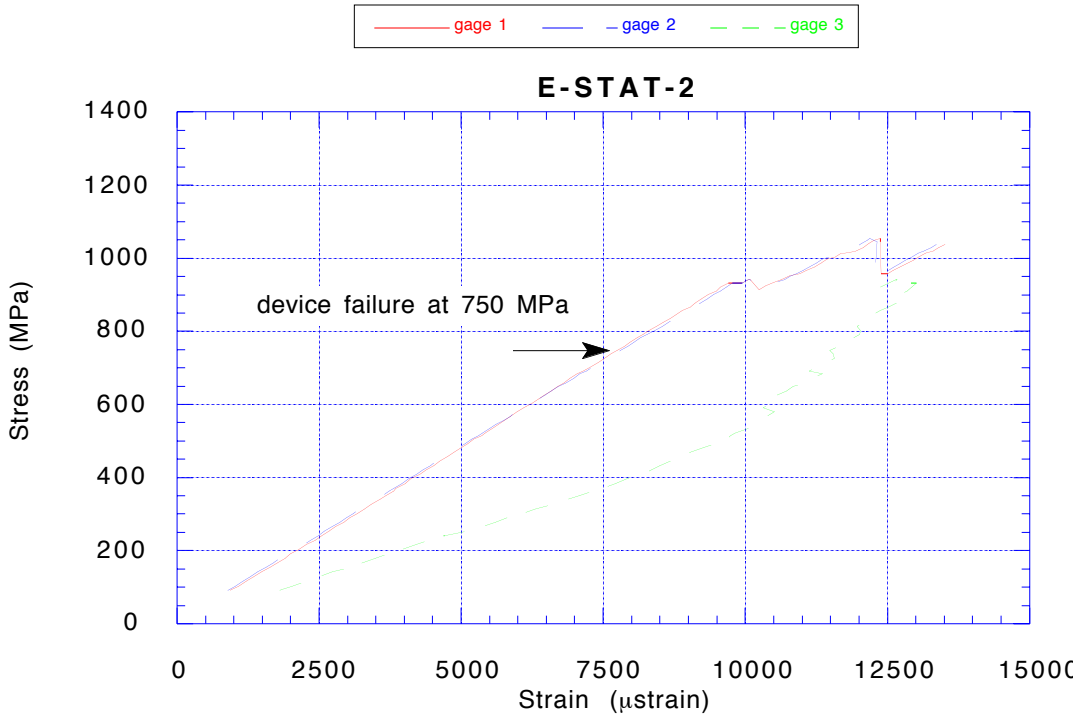


Figure 3.13b **Stress-strain curves of static tension test article E-STAT-2.**

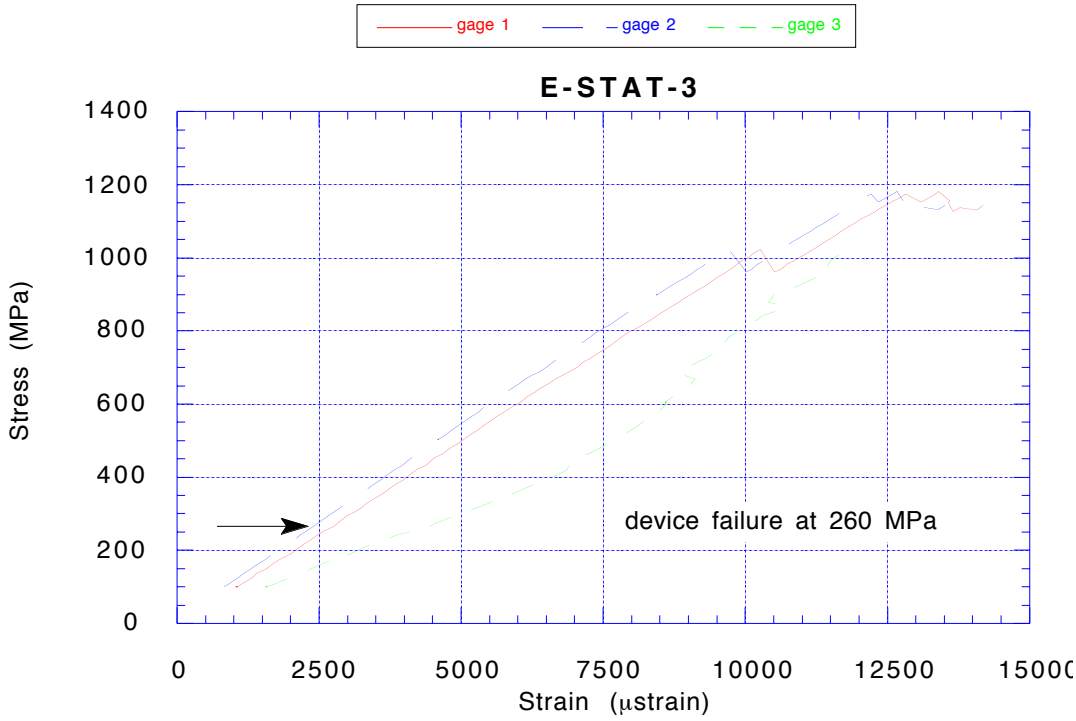


Figure 3.13c **Stress-strain curves of static tension test article E-STAT-3.**

Also shown on the plots in Figure 3.13 are three longitudinal stress-strain curves of each of the test articles. The strain values are those from the strain gages 1, 2, and 3, placed as shown in Figure 3.9, while the stress values were computed by dividing the applied load by a nominal cross-sectional area of 5.4×10^{-5} m^2. In all cases, the longitudinal strain measured to the side of the chip and that measured in the far field are close, while the strain measured directly over the chip shows a strain concentration of from 1.6 to 2.3, with a variation possibly due to the difficulty of repeatability in the placement of the gage directly over the chip. These results suggest that the disturbance in the otherwise uniform stress and strain fields caused by the inclusion of the chip is a very localized one and that the ratio of coupon width to device package width of approximately 5.3 :1 was sufficient to exclude significant interaction between the strain in the vicinity of the chip and the strain near the free edges

of the coupon.

The stress-strain plots from the static tensile tests of the two test articles with the RTV silicone isolation layer, R-STAT-1 and 2, are shown in Figure 3.14. The overall appearance of these curves is similar to those obtained from the tests of test articles with the standard epoxy layer shown in Figure 3.13. The comparison of the strain measurements from the gages directly over the embedded device location with those from the gages further away shows localized strain concentrations of 1.8 and 1.9 over the device, also similar to those observed in the previous tests.

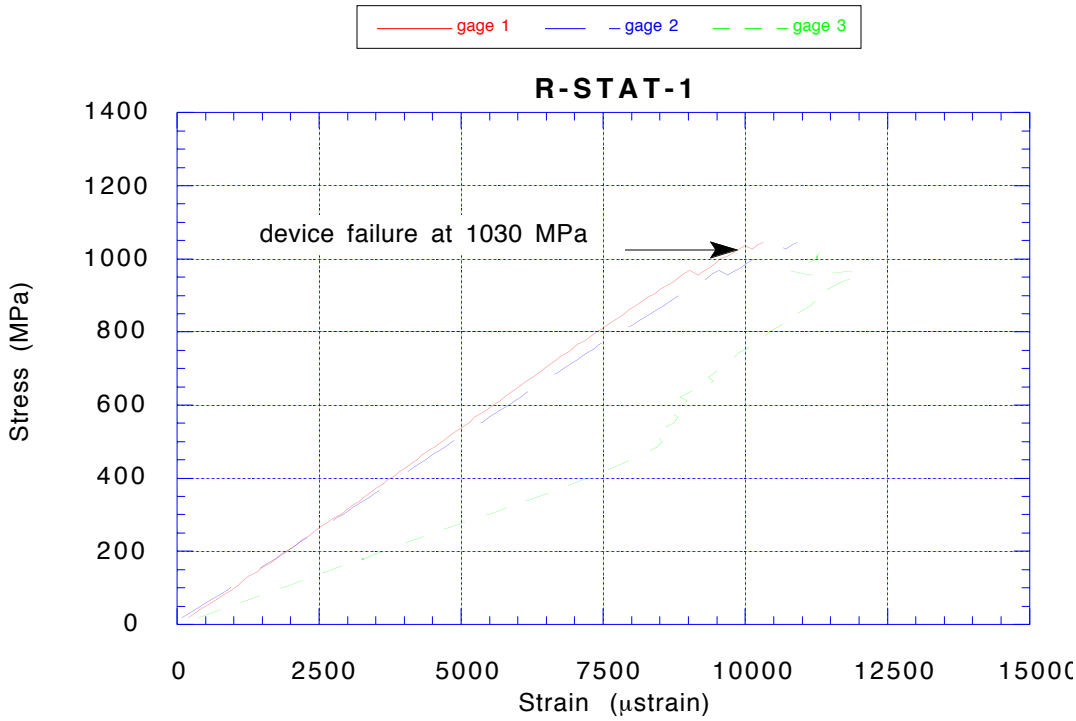


Figure 3.14a **Stress-strain curves of static tension test article R-STAT-1. Longitudinal strain at three locations is shown along with the load level at which transistor function ceased.**

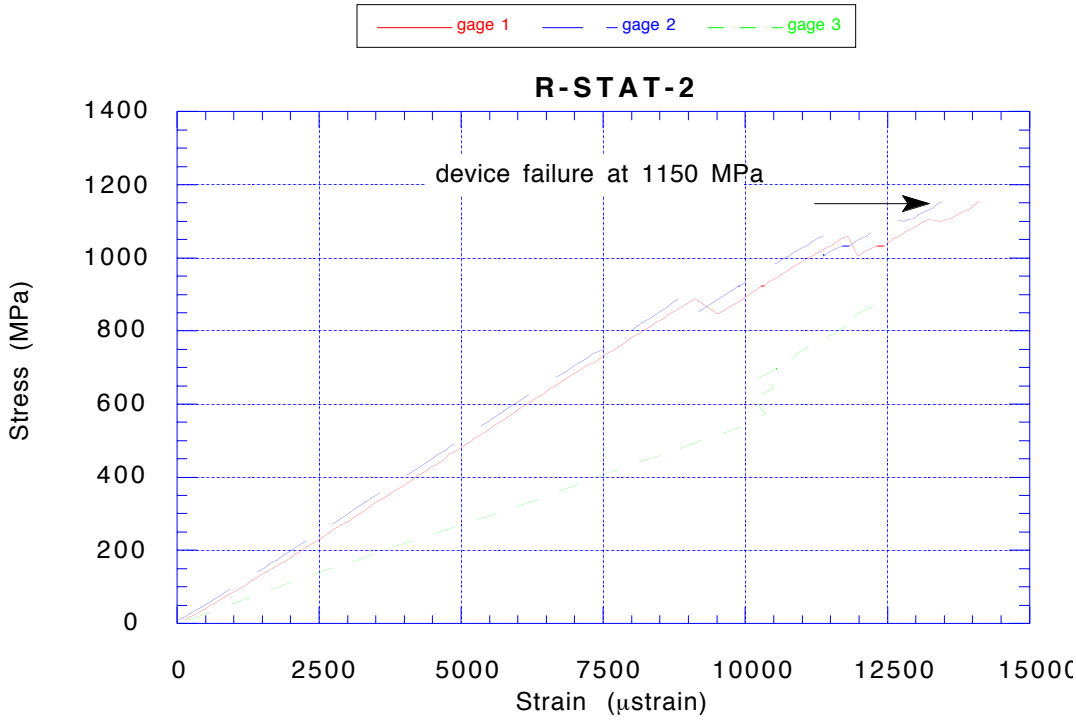


Figure 3.14b **Stress-strain curves of static tension test article R-STAT-2.**

As mentioned in the description of the mechanical test procedures (Section 3.3.1), the static tests of test articles with the RTV silicone were halted shortly after the devices ceased to function in order to allow direct examination of the chip and leads. In the case of R-STAT-1, damage to the surface 0° ply was visible when the test was halted after device failure, indicating that complete structural failure was immanent. The device functioned up to 9900 μstrain and 1030 MPa, 96% and 98% of the maximum values of 10300 μstrain and 1050 MPa. The test with R-STAT-2, however, did proceed to the point at which the load dropped greatly (to near zero); the device functioned up to 100% of the maximum values of 14200 μstrain and 1150 MPa.

The devices embedded in both test articles with the RTV silicone functioned at load levels greater than those reached in any of the tests of test

articles with the epoxy layer. This suggests that although it did not completely enclose the chip, the RTV layer was in fact successful in performing its mechanical isolation function and alleviating the stress concentrations causing damage to the chip or its leads. No other noticeable changes were observed in the appearance or mechanical behavior of the coupon as a result of the difference in protective layer, aside from the previously mentioned 7% increase in coupon thickness at the embedded device location.

Because of the fragility of the chips and leads without the standard epoxy layer, the preparation of the test articles with the RTV silicone was rather difficult, and only a few were produced. In view of the apparent success of the RTV silicone in the static tests, the originally planned third static test was abandoned, and the last mechanical test article with the RTV silicone was instead employed in a cyclic test.

The results of the static mechanical tests are summarized in Table 3.2. As previously noted (Section 3.2.4), three trial cures were performed using the standard 350 F TELAC cure for AS4/3501-6 before switching to the modified 300 F cure schedule. Maximum stress and modulus data for some coupons from these trial cures have been included in the table for comparison. Of these test articles, two included an embedded (though non-functioning) device, and two were essentially blanks with the $[0°/90°/0°_2]_S$ layup but with neither the embedded device nor the modifications (holes and slots cut in interior plies) necessary to accommodate a device.

Test article type	Device Failure		Laminate Maximum		Long. Elastic Modulus E_L (GPa)
	Strain (μstrain)	Stress (MPa)	Strain (μstrain)	Stress (MPa)	
E-STAT-2	7700	750	13500	1050	97
E-STAT-1	9000	1010	14000	1220	113
E-STAT-3	2300	260	14200	1180	101
R-STAT-1	9900	1030	10300	1050	109
R-STAT-2	14200	1150	14200	1150	99
NFD-STAT-1	-	-	-	1270	108
NFD-STAT-2	-	-	-	1310	117
ND-STAT-1	-	-	-	1420	105
ND-STAT-2	-	-	-	1630	113

Table 3.2 **Comparison of results from static extension tests of test articles with and without RTV silicone isolation layer, as well as standard cure coupons with and without embedded devices.**

It should be noted that among the four samples with the standard cure, the presence of the device appears to have had no effect on the longitudinal elastic modulus, though the maximum stress is decreased by some 15%. The use of the non-standard cure described above shows an additional reduction in maximum stress of about 10% and a decrease in modulus of 5%. The large scatter in the measurements and the small size of the samples make these values rather tentative. Considering that in the vicinity of the embedded device half of the plies (4 of 8) and two thirds (4 of 6) of the 0° axial load bearing plies are interrupted, this is a modest reduction in strength.

The cyclic tests described in Section 3.3.2 were performed on test articles like those used in the static tests; three had the standard epoxy layer (E-CYC-1, 2, and 3) and one had the RTV silicone isolation layer (R-CYC-1). The test articles were subjected to tension-tension loads varying sinusoidally between 10% and 100% of a maximum stress level, which was set to roughly 40-50% of

the laminate failure stress. This level was intended to be high enough to provoke fatigue failure of the devices; it induced strain levels much higher than the usual 2500 μstrain limit for composites. The transistor failure behavior was similar to that observed in the quasi-static tests; the nominal characteristic curve was abruptly replaced with a flat line, though in the case of the test articles which completed more than a single cycle, this was an intermittent condition appearing under load and returning to normal or near normal upon the removal of the load.

Of the test articles with the standard epoxy layer, two failed before the completion of even a single cycle, and one failed after completing four cycles. As the early loading cycles of all tests were performed with long periods, it was possible to record the loads at which these failures occurred, and they are presented with the other test results in Table 3.3. In the case of E-CYC-1 and E-CYC-2, the failure had an intermittent characteristic, in that the transistor curve regained its proper shape, although with a reduced I_{DS}, when the load was removed. Test article E-CYC-3 remained inert after failure, even when the test article was unloaded.

Test Article Designation	Peak load (MPa)	Device Failure Cycle	Device Failure Load (MPa)
E-CYC-1	540	1	270
E-CYC-2	540	4	530
E-CYC-3	420	1	210
R-CYC-1	420	123	-

Table 3.3 **Comparison of results from cyclic extension tests on test articles with standard protective epoxy and with RTV silicone isolation layer.**

As was the case with the static tests, the test article with the RTV

silicone exhibited a greater tolerance for mechanical loading, failing only after a total of 123 cycles. This test article showed an intermittent failure similar to that of E-CYC-1 and E-CYC-2. In post-failure tests, it was observed that the transistor characteristic curve returned completely to its nominal form when the test article was unloaded. When the load was reapplied and slowly increased to around 160 MPa, the curve was replaced by the flat line; after a few seconds or minutes the curve would begin to reappear intermittently, becoming more distinct and approaching its nominal form, as illustrated in Figure 3.15.

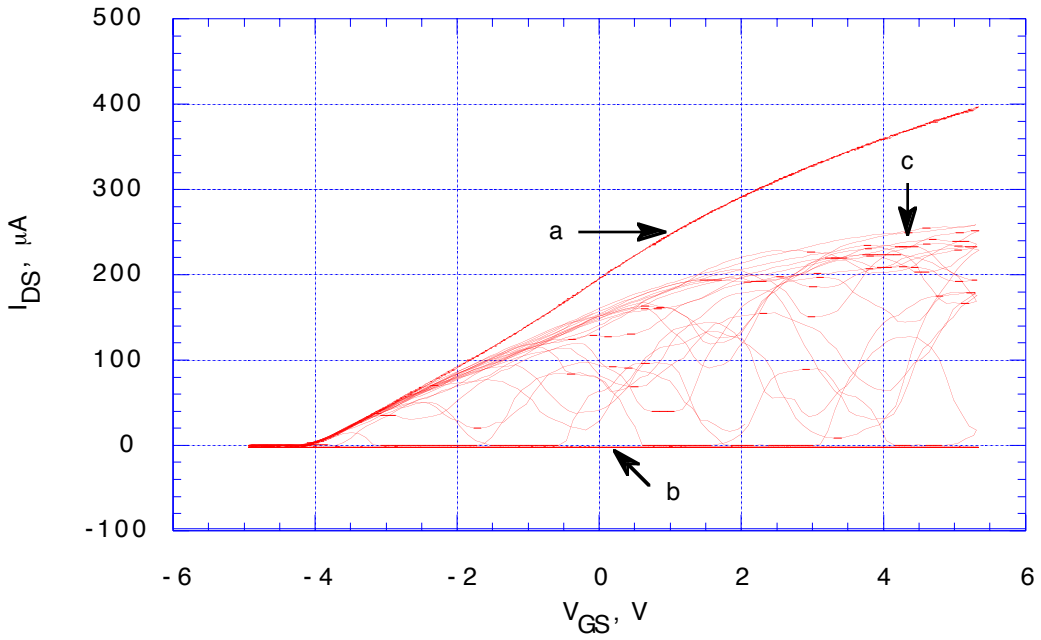


Figure 3.15 **Transistor characteristic curves of R-CYC-1 during cyclic test. Curve (a) shows the nominal, undamaged behavior; flat line curve (b) shows loss of detectable current under load after fatigue failure; curve (c) shows gradual recovery of transistor behavior during relaxation under tension.**

Based on the information gathered from these mechanical tests, it appears that the failure mode of the device is almost certainly one of lead breakage or lead debonding. This conclusion is based on experience gained

during the curing process, interpretation of the transistor characteristic curve traces and supporting measurements of diode drops across leads, and direct examination of cured and uncured devices.

Failure of the devices in all static tests was abrupt and unmistakable; the typical transistor characteristic curves appeared to instantly change during the loading ramp to be replaced by flat lines. This would be consistent with breaking of the drain or source leads, with the shearing off of the oxide and metal layers on the silicon chip, or with the fracture of the silicon chip itself. In all cases but one, the chips in these tests were destroyed along with the coupons, so that these possibilities could not be distinguished.

In the case of R-STAT-1, though, the test was halted before the complete fracture of the coupon. Some pairs of leads, which normally would show either low resistance conduction or a diode drop, showed open circuits, but it was possible to measure a conduction current between the leads to the common drain and the source of the device's signal transistor. These results are consistent with the interpretation that the chip and its structures remained intact, but that most of the leads had broken or debonded. Had the chip itself or the oxide or metal layers broken, it is unlikely that any leads would have shown anything other than an open circuit.

The results obtained from the cyclic tests also are consistent with the presence of a lead failure mode. The intermittent nature of the failures observed would hardly have been possible had the chip or its structures broken. The integrity of the field effect transistor, once violated by the physical fracture of the silicon or by the shearing off of the gate oxide or metallization layers, could not have been restored by simply bringing the fragments back in to contact by removing the load. Such a renewal of

function could, however, be the result of bringing back into contact the two ends of a fractured lead, or the end of a debonded lead and its bonding pad. In these cases, the situation is merely that of a faulty connection; when the two metallic part are reconnected, the circuit functions as it should.

The curves obtained from the cyclic test of R-CYC-1 shown in Figure 3.15 may be explained by the presence of lead breakage or debonding. When the connection to the transistor drain or source is solid, curve (a) results; when it is completely broken, curve (b). The gradual recovery of the signal under load, curve (b), may be the result of the creep of the RTV silicone layer; as it relaxes, the metal parts are brought back into contact. In the cyclic tests of E-CYC-1 and E-CYC-2, it was noted that the curve which reappeared upon unloading had the general form of the nominal behavior, but showed a reduced I_{DS}. Since the device was operated at a constant V_{DS} of 10 mV this could be interpreted as an increased resistance, possibly due to the plastic deformation of a copper drain or source lead, or to a reduced contact area either between two broken ends of a lead or between a lead and its contact pad.

In order to gain further insight into the possible cause of device failure, direct examinations were made of several embedded devices, specifically E-CYC-1, R-CYC-1, and R-STAT-1, as well as of a device which had failed during an unmodified, high temperature cure as described in Section 3.2.3. In each case, the test article was soaked for several hours in concentrated nitric acid to etch away the greater part of the surrounding structural epoxy. When the surface of the chip was largely exposed, a methyl ethyl ketone (MEK) solution was used to soften the protective epoxy layer, which was then carefully removed under a microscope with use of small picks and brushes. In the case of the devices with the RTV silicone layer, a mixture of methylene chloride,

methanol, and toluene (5f5 from Sterling-Clark-Lurton Corp.) served the same purpose.

In all of the examinations the silicon chip itself appeared to be intact. In test articles E-CYC-1 and R-STAT-1, several leads were observed which had apparently become bonded from the chip. The device in test article R-CYC-1 showed both loose bonds and cracks completely severing some of the leads. The fact that the apparently debonded leads were intact and unbent would seem to be indicative of damage occurring before the stripping for examination; otherwise the delicate copper leads would have been deformed. The examination of the failed device cured according to the standard cure schedule also revealed two partially cracked leads, as well as one debonded lead. The appearance of a typical crack is shown in Figure 3.16.

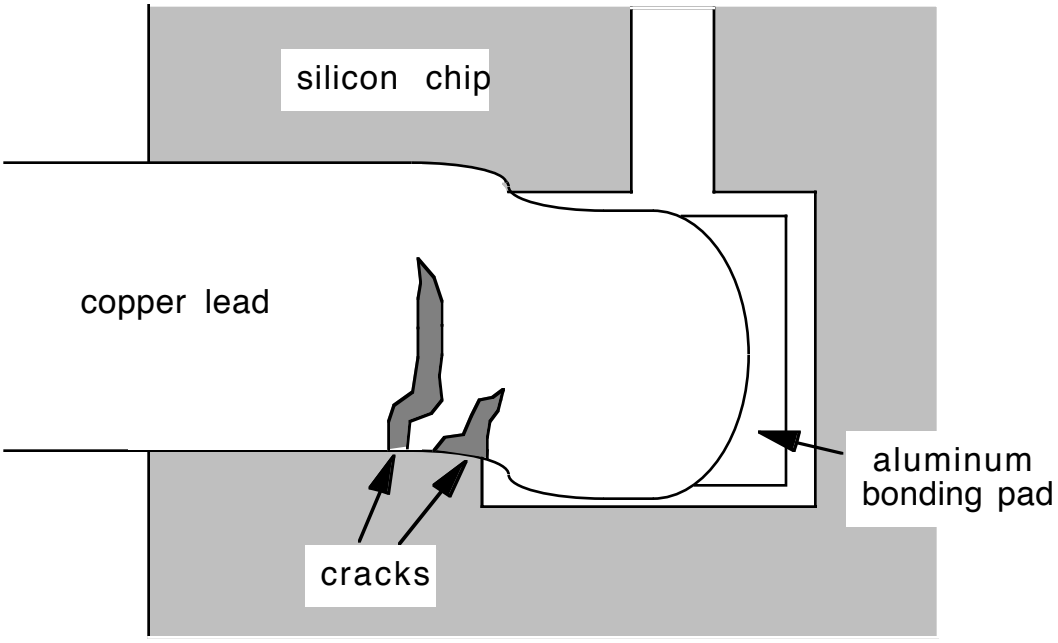


Figure 3.16 **Illustration of location of typical crack in copper lead near bond to chip. Examination was performed on unembedded chip.**

Since the damage observed could have been incurred during the removal of the surrounding epoxy, an examination was also made of some

devices before embedding, both with and without the standard protective epoxy applied by the manufacturer. In both cases, cracks were found in the leads similar to those observed in the test articles. These observations tend to support the idea that the leads were the weak link in the mechanical tests as well as during the cure, especially in view of the pre-existing flaws, which might well account for both the static and cyclic test articles which failed at low load levels.

In this section, the procedure and results of mechanical tests of the embedded devices were described. The static tests of the test articles with the standard protective epoxy showed a degree of success for the method for embedding described in Section 3.2. The devices were insensitive to the increasing applied load until failure, which occurred in one case as low as 22% of the maximum coupon load. Indirect evidence and direct examination indicated lead cracking or debonding (or both) as the most likely device failure mode.

The test articles with the RTV silicone isolation layer proved more durable, suggesting that the isolation layer was successful in relieving strain transfer to the leads and chip and thus postponing device failure to load levels at which the composite coupon itself completely broke. This layer was also effective in increasing the number of cycles withstood in the cyclic tests from 4 or fewer to 123. Though the number of tests was too small to yield statistically reliable values for reliability predictions, they were sufficient to demonstrate the success of the embedding technique, the device failure mode, and the effectiveness of a means for combating that failure mode.

3.4 Temperature-Humidity-Bias Test

The remaining test performed on the embedded devices was a temperature-humidity-bias (THB) test. The devices were subjected to a high temperature, high humidity environment while being operated at a constant operating point or bias. The purpose was to check for changes in transistor behavior as an indication of corrosion due to excessive moisture absorption or ionic contamination from the structural epoxy. Conventionally packaged control devices were tested concurrently for comparison of results to the reliability of commercially available products.

3.4.1 Procedure description

This test was performed on three test articles THB-1, 2, and 3, the manufacture of which was described in Section 3.2. The test articles were placed in a Blue M AC-7402HA-1 environmental chamber which was equipped to maintain a constant temperature of 80 C (176 F) and a constant relative humidity of 80%. The flexible copper/Kapton leads of the test articles, which were run between the door and the wall of the chamber without significantly disturbing the chamber seal, were attached to test circuits which provided the necessary support both to monitor I_{DS} under constant bias conditions and to record transistor characteristic curves such as the one in Figure 3.12 at intervals spaced roughly logarithmically in time, according to the schedule shown in Figure 3.17. The entire test lasted for 7500 minutes (125 hours), not counting the hour required to bring the chamber temperature and humidity up to the specified test conditions.

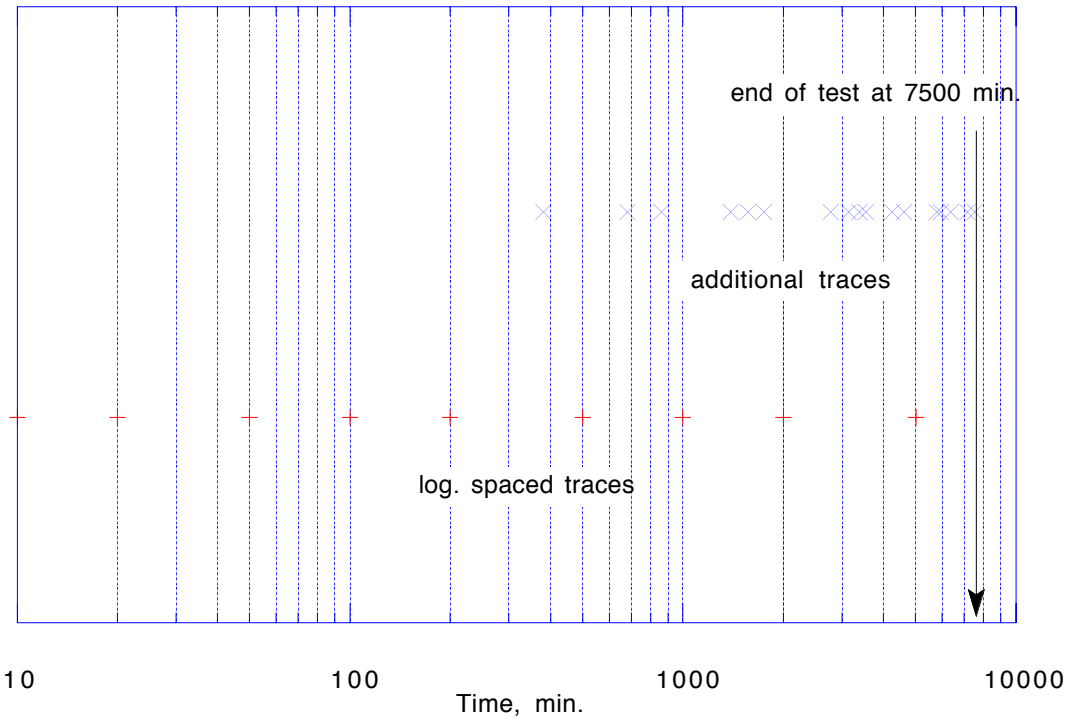


Figure 3.17 **Plot of the times at which transistor characteristic curves were recorded during the THB test.**

Since the later intervals between curve measurements became rather long, supplementary curve records were taken at convenient times during the day. At all other times, the constant bias transistor behavior was monitored by means of the strip chart recorder as described previously.

Although the purpose of this experiment, like the others, was not to establish statistically valid estimates of such performance characteristics as mean lifetime, but rather to seek out possible failure modes, it was deemed sensible to include in the test a means of providing some measure of comparison with commercial devices. To this end two control devices were tested along with the embedded devices. As the closest analog to the devices under test, a MOSFET in a plastic package, was not available, the controls chosen were a junction FET (JFET) in a plastic package and a MOSFET in a

hermetically sealed metal package. The JFET was a 2N-5459 n-channel depletion mode device in a TO-92 type package, and the MOSFET was a 2N-4351 n-channel enhancement mode device in a TO-72 type. The characteristics of these devices being somewhat different from those of the embedded devices, the constant bias values of V_{GS} were -1 V and 5 V for the 4351 and the 5459, respectively, in order to obtain I_{DS} levels comparable to those obtained with a bias of +1 V on the embedded devices. In the case of the 5459, the V_{GS} triangle wave generator was also increased in amplitude to range from approximately -7 V to +7 V so that a more complete characteristic curve could be traced.

As the strip chart recorder used had only four channels, the 5459 was continuously monitored, as its plastic packaging was more similar to that of the embedded devices. The 4351, being hermetically sealed, was expected to be the least likely to exhibit behavior changes during the test, and so was not continuously monitored. A separate circuit was, however, used to supply the constant bias values of V_{GS} and V_{DS} for maintaining current flow during the test. When constant operation was interrupted to take characteristic curves, the traces of both the 5459 and 4351 devices were recorded.

3.4.2 Results

Of the five devices employed in the THB test, the two control transistors and THB-1 showed no change in their function. The remaining two embedded devices, though, showed changes in both their curve traces and strip chart records of their drain-source currents at the constant operating point at which they were maintained during the test. These deviations will now be described.

THB-2 exhibited the anomalous transistor curve (b) shown in Figure

3.18. This change was first noted in the trace recorded at 860 minutes into the 7500 minute test, and could be reproduced by testing the same device on another curve tracing circuit, showing that the effect was a change in the device, not merely a problem with a specific testing circuit. The change was intermittent and the curve returned to normal a few minutes later. The anomaly reappeared in the traces recorded at 3140 and 3540 minutes. At 3540 minutes, measurements were made with the diode indicator of the multimeter of the voltage drops appearing at several leads with respect to the substrate. Each voltage drop during the appearance of the anomaly was slightly elevated above the value measured during normal operation of the device, and above the corresponding values measured on another properly operating test device. The anomaly was not observed in later traces.

Comparison of the anomalous curve (b) with the nominal curve (a) in Figure 3.18 shows, in addition to the obvious hysteresis and substantial non-zero current for V_{GS} below the threshold voltage, a slight elevation of I_{DS} when the transistor is turned on. Since the constant bias operating point during the test held V_{GS} at 1 V, this change was also faintly visible on the strip chart. Although a change of this small magnitude in the trace could also be caused by electrical interference by nearby machinery, periods of what appeared to be elevated I_{DS} occurred intermittently throughout the trace for this device during the test, the earliest beginning at 275 minutes and lasting for about 12 minutes.

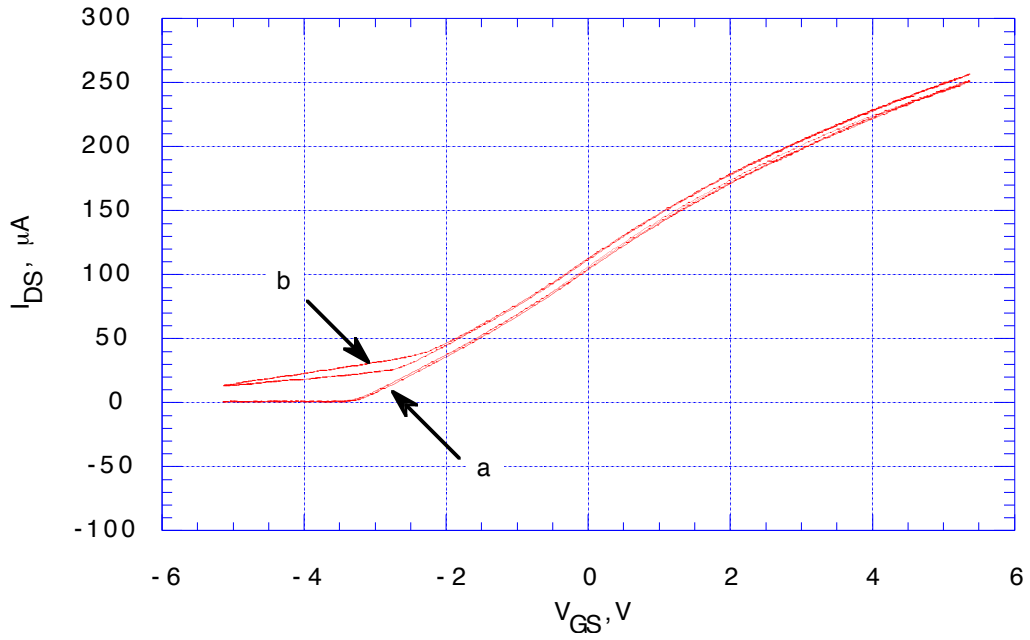


Figure 3.18 **Transistor characteristic curves of THB-2 860 minutes into the test. Curve (a) shows nominal operation; curve (b) shows the curve obtained during the appearance of the intermittent anomaly described in the text.**

The aberrant behavior in the other malfunctioning device, THB-3, was first visible on the strip chart recorder at 7290 minutes, as illustrated in Figure 3.19. When the substantial and accelerating drop in I_{DS} was observed, the chart was interrupted to record a characteristic curve and voltage drops, as well as to show that the effect could be reproduced on another test circuit. The anomaly was reproducible; the curve trace had the same form as the nominal operation, showing a sharp cut-off at the threshold and no hysteresis as observed in THB-2, but showing a reduction in I_{DS} consistent with that reflected in strip chart. The voltage drops measured were all nominal except for that from the drain to the substrate, which was substantially elevated.

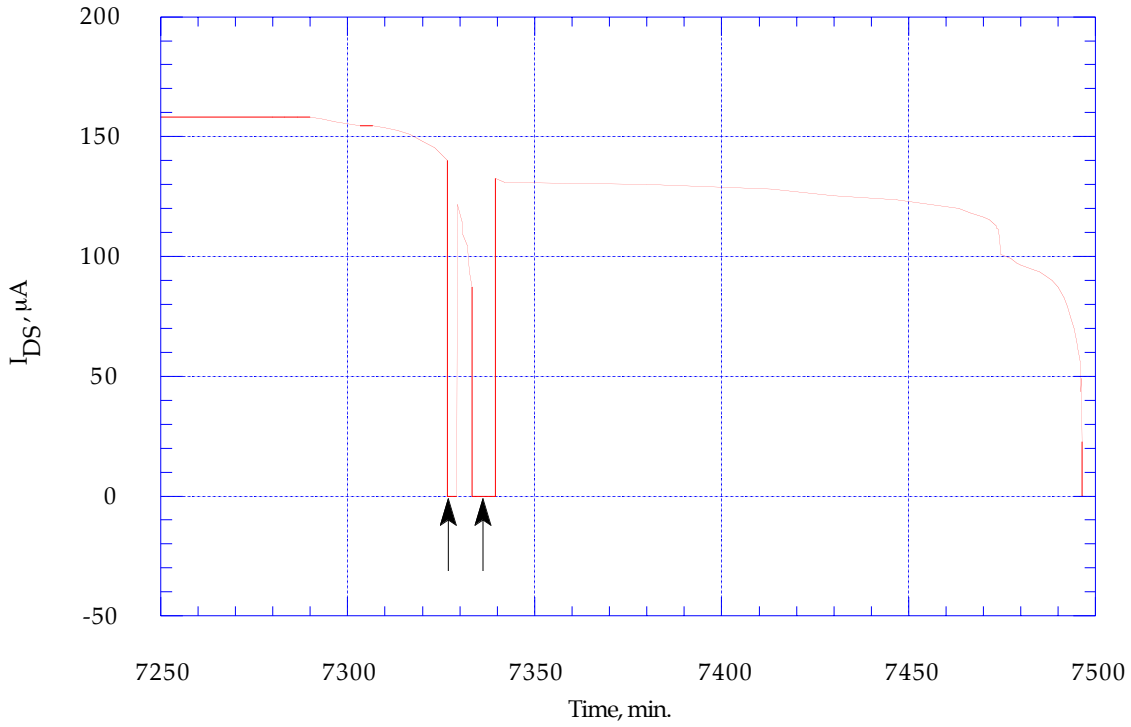


Figure 3.19 **Time history of source-drain current for THB-3 near the end of the THB test. Decay of I_{DS} under constant operating conditions is consistent with gradual degradation of the copper-aluminum bonding of the drain or source leads. Gaps at arrows indicate points at which strip-chart was disconnected and curve traces were taken.**

Both of the anomalies described above could be accounted for by degradation of one or more lead bonds. In the case of THB-2, the elevated voltage drop readings for all leads with respect to that attached to the substrate suggests that the substrate lead itself was faulty. This was supported by later experimentation by attaching a normal, unembedded device to a curve tracing circuit but leaving the lead bonded to the substrate disconnected from the reverse-bias voltage source, thus simulating the effects of a discontinuity in the substrate lead; a curve similar to (b) in Figure 3.18 was produced. Fracture of the copper lead itself seems unlikely, since any thermal expansion (and attendant strain) of the test article would have been completed during the warm-up, long before the fault appeared. Lead stress could, however,

have been due to a slow absorption of moisture by the test article. Another possible explanation would involve some corrosion mechanism at the junction of the copper lead and the aluminum bonding pad. Progressive degradation of this connection could have interrupted the substrate biasing, while crumbling and shifting of the remaining parts of the copper lead could explain the intermittent nature of the anomaly.

A similar explanation may be invoked to account for the behavior of THB-3. In this case, the voltage drop measurements clearly indicate a problem with the lead or bond associated with the MOSFET drain. Degradation of this connection could manifest itself as an apparent increase in resistance; in the presence of a fixed V_{DS}, this would be translated in to a proportionally reduced I_{DS}. The gradual onset of this condition as shown in Figure 3.19 is consistent with a progressive corrosion of the copper-aluminum bond. The partial recovery at 7340 minutes and the pause at 7475 minutes may be due to the crumbling and shifting suggested as an explanation for the intermittent nature of the behavior of THB-2.

A direct inspection like that described in Section 3.3.2 was made of the devices in test articles THB-1, 2, and 3. Articles THB-2 and 3 both exhibited several weak or broken bonds, and THB-3 also had noticeable cracks across some of its leads. The leads of THB-1 also seemed to be rather fragile, possibly indicating a degree bond degradation prior to the stage at which electronic behavior is affected.

In this section, the procedure and results of temperature-humidity-bias tests of the embedded devices were described. Two of the three devices tested showed anomalous behavior before the end of the 7500 minute test, while the third test article and both control devices showed no deviations in function.

The behavior of the failed devices was consistent with corrosive damage to the leads or lead bonds, and weaknesses were observed in these areas by direct inspection of the devices. This suggests that reliability could possibly be improved by thickening the fragile copper leads and strengthening the bonds, which would also be likely to improve the performance of the devices under mechanical loads.

CHAPTER 4:
SINGLE-CHIP MICROCOMPUTER CONTROL

The arguments in Chapter 2 addressed some of the basic considerations regarding the processing architecture of a distributed control system. Chapter 3 presented work demonstrating a method for physically embedding electronic processing components. The applicability of the arguments in Chapter 2 and the method of Chapter 3 depend on the level of functionality attainable with the smallest number of chips. This chapter examines some of the capabilities of a single-chip microcomputer, and as such is a natural extension of the previous discussion.

It was suggested in Chapter 2 that physically embedding distributed processing components in the structure could simplify connection to embedded sensors and actuators, protect the components from possible damage, and provide the structure with a clean surface. In the Chapter 3, the development of a technique for embedding electronic devices in composite structures was described. Tests of the survivability of the embedded devices under mechanical stress and in a high temperature, high humidity environment were also presented. The results of this work showed that physically embedding the electronic components of the control system of an intelligent structure is feasible.

At the same time, the advantages of embedding electronic components must be weighed against the effects of such inclusions on structural integrity. The arguments for developing an embedding technique causing the least interruption to composite plies also suggest that the number of inclusions be kept to a minimum. This has important implications for processor

architecture. In contrast with conventional computer control systems which employ many specialized chips to perform the various functions of signal conversion, computation, storage, and communication, the embedded control system of an intelligent structure would greatly benefit from the use of processors which could combine as many functions as possible on a single chip. This would greatly simplify the interconnections as well as reduce the adverse effect on structural integrity.

The work described in this chapter demonstrates some of the capabilities of an existing single-chip microcomputer in controlling the vibrations of a simple structure. The plant with its attendant actuators and sensor will be described and a mathematical model of the plant behavior will be presented. This will be followed by a discussion of the characteristics of the microcomputer controller used in the closed-loop experiments. The derivation of the control strategy and predictions of its performance based on mathematical models of the various components will be presented. These predictions will be compared with actual data from closed-loop experiments.

4.1 Description of the Experimental Setup

The demonstration of single-chip microcomputer control capabilities required an experimental set-up with a number of desirable elements. Among these were a simple structure, a sensor/actuator pair which might be typical of an intelligent structure, a source of disturbance excitation, and a means of evaluating the control system effectiveness through some performance measure. In this section the physical characteristics and mathematical modelling of the plant will be described, but first an overview of the setup including the control loop and the data gathering equipment will be presented.

Figure 4.1 shows a schematic of the setup used in the control experiment. The simple structure takes the form of a cantilever beam which has bonded to it two pairs of piezoelectric ceramics. These piezoelectrics, typical of the actuator mechanisms proposed for intelligent structures, serve to apply both control effort and disturbance to the beam. The disturbance is introduced in the beam by applying a voltage to one pair of piezoelectric ceramics, and the resulting motion of the beam tip is detected by a displacement sensor. Although the sensor, which measures deflection with respect to a fixed stand, is not truly typical of a sensor which one would expect of an intelligent structure, it was part of the existing equipment suite, and had the advantage of providing a meaningful measurement for performance evaluation. The tip displacement might for example be considered to be a measure of shape control or general vibration disturbance levels, either of which could be of interest in a precision controlled intelligent structure.

In closed-loop operation, the control computer uses the information from the sensor information to generate a signal which, when amplified, is applied to the other pair of piezoelectric ceramics to reject the disturbance. A Tektronix 2630 data acquisition system is used to both generate the random disturbance signal and record the response of the displacement sensor. This allows the characterization of the transfer functions of individual components of the setup, as well as measuring the behavior of the entire system in both the frequency and time domains.

This section describes the details and characteristics of the cantilever beam plant with its actuators and sensor. A short explanation of the piezoelectric effect will be presented, along with the beam transfer functions measured from each actuator to the sensor. The generation and refinement of a mathematical model of the plant will also be described.

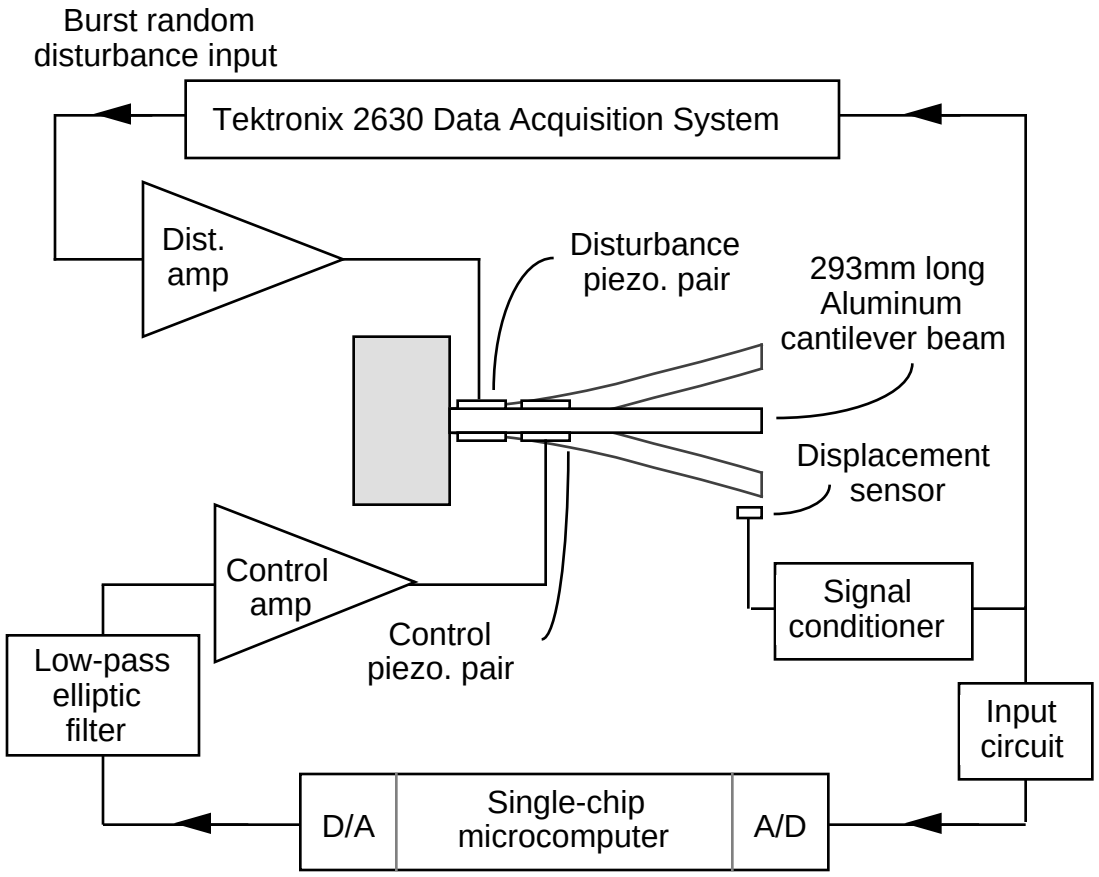


Figure 4.1 **Schematic of setup for single-chip microcomputer control experiment. Shows beam plant, actuators, sensor, and feedback loop components.**

4.1.1 Actuation, sensing, and dynamic measurements

Figure 4.2 shows the plant to be controlled. The beam with its actuators and sensor was a test article used previously in work at the Space Engineering Research Center [20]. Manufacture of the test article involved bonding pairs of piezoelectric ceramic plates to the surface of the beam, clamping the beam in a heavy mount to provide a cantilever end condition, and constructing a stand for the displacement sensor.

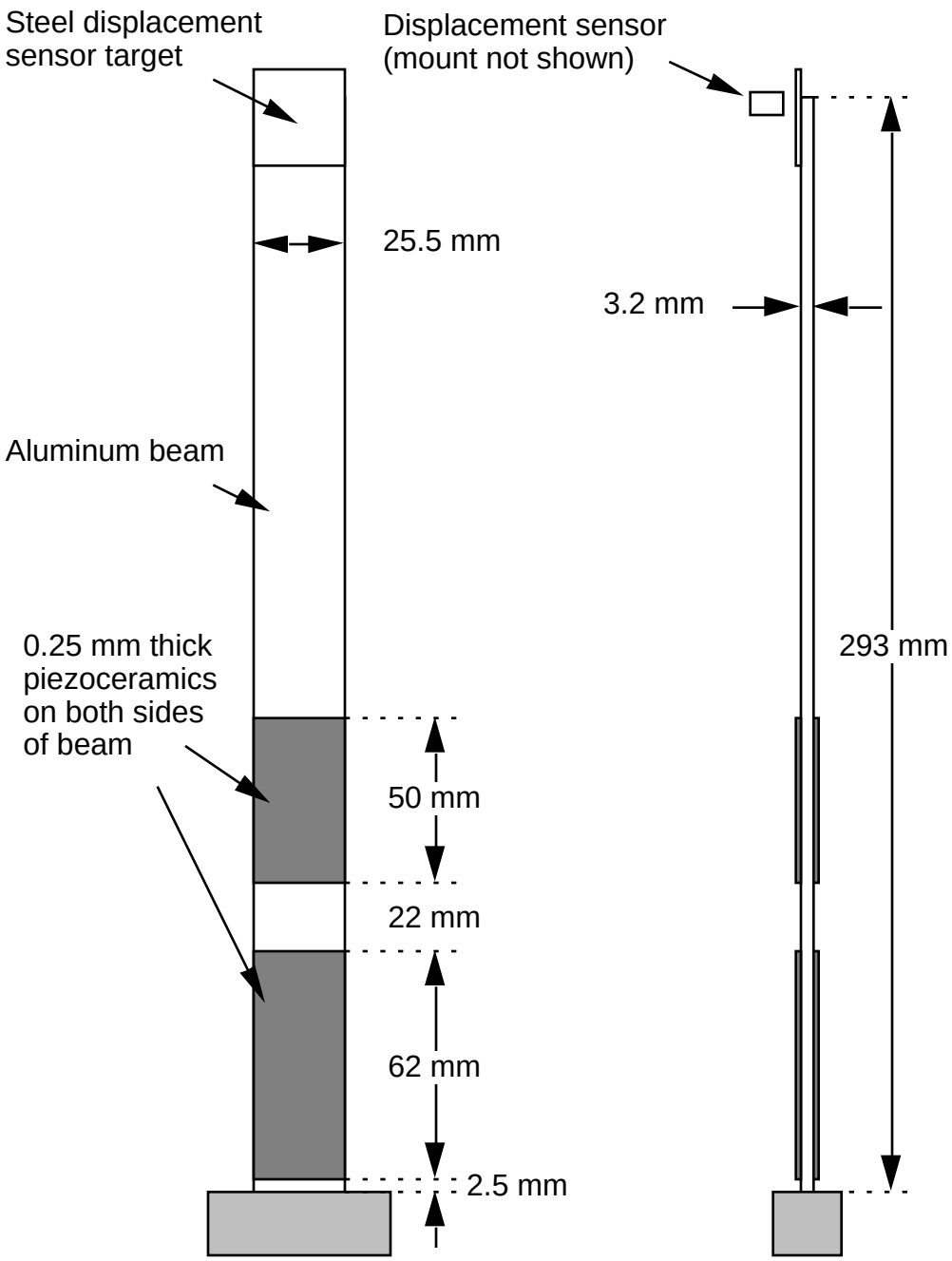


Figure 4.2 **Dimensions of cantilever beam showing location of actuators and sensor.**

The piezoelectric effect and its use in causing beam bending is illustrated in Figure 4.3. When a voltage is applied to the electrodes of a piezoelectric ceramic to produce an electric field opposite the poling direction, a deformation is produced as shown: the ceramic contracts in the poling

direction and expands in the other two directions. Reversing the voltage and electric field produces the opposite deformation. In this way, the proper orientation and excitation of two ceramic plates bonded to the sides of a beam can, by expanding on one side and contracting on the other, produce the bending effect shown.

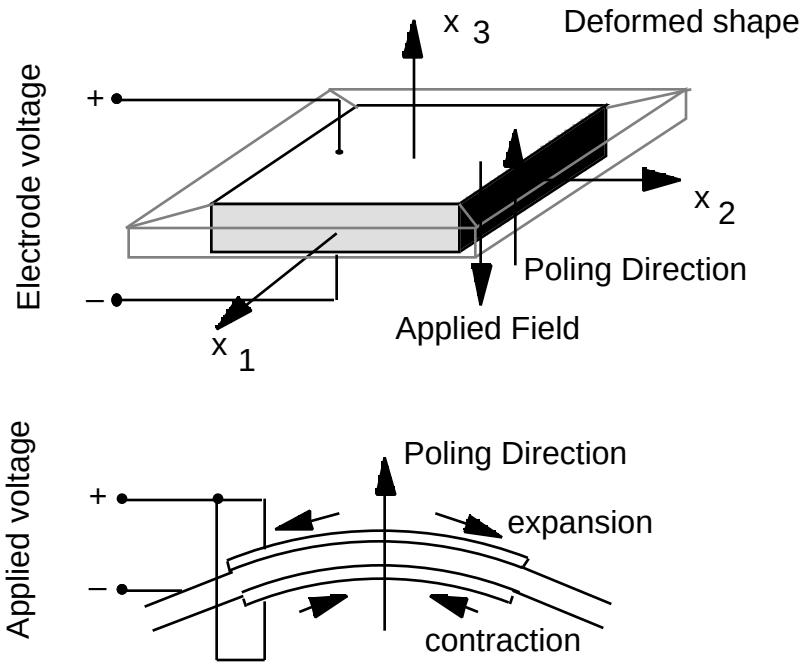


Figure 4.3 **Illustration of the piezoelectric effect. Applying an electric field to a piezoceramic produces strain deformations, which can be used to induce bending in a beam.**

The piezoceramic elements used in this experiment were of the G-1195 type manufactured by Piezoelectric Products, Inc. They were bonded to the aluminum beam by a thin layer of conductive epoxy, with the poling directions aligned so that the application of the same voltage to the exposed electrodes with respect to the electrically grounded beam produced the expansion/contraction action shown in Figure 4.3, yielding bending of the beam.

Each pair of piezoceramics was driven by a power amplifier

incorporating an Apex Microsystems PA08V high voltage op-amp. These amplifiers were operated at fixed gains throughout the experiments; the amplifier for the disturbance piezoceramic pair produced a DC gain of 9.90 with a -3 dB point at 10.7 kHz, and the amplifier used to drive the control actuator pair had a DC gain of 20.51 with a -3dB point at 15.7 kHz. These gains and corner frequencies were measured with the amplifiers connected to the piezoceramics, in order to include the effects of lead resistance and capacitive load.

The motion of the beam tip was measured by a Bently-Nevada 7200 series 11 mm diameter position sensor. This was mounted on a stand near the tip of the beam, essentially providing an inertial position reference, and producing 1.83 V/mm. The position sensor and stand, like the beam itself, were part of an existing apparatus. While such a sensor could not be used in an intelligent structure with a completely embedded control system, similar information could be obtained by integrating the signal from an embeddable accelerometer. Strain information could also have been used, either alone or in combination with acceleration and its integrals.

The transfer functions obtained by exciting each pair of piezoceramics and measuring the tip deflection are presented in the next section, along with those obtained from a mathematical model of the system.

4.1.2 Mathematical model of the plant

The development of a state-space model of the beam with its actuators and sensor was presented in [20]. This model was based on a Rayleigh-Ritz formulation in which the assumed shapes were taken to be the first five exact cantilever Bernoulli-Euler beam mode shapes augmented by two static deformation shapes. The static shapes were those obtained by applying

constant voltages independently to each pair of piezoceramics. This helped to account for the effects on the true mode shapes of the discontinuous beam stiffness due to the presence of the piezoceramics. The modal forcing matrix was obtained by including the piezoelectric effect in the virtual work statement, so that the matrix yielded the effect on each mode of applying voltages to the pairs of piezoelectrics.

The overall magnitude of the model transfer functions was scaled to match the experimentally observed transfer function magnitudes at 10 Hz, about 30% of the lowest resonant frequency. This adjustment served to account for the effects of the tip displacement sensor conversion factor, the piezoelectric amplifier gains, and any deviation from piezoelectric effectiveness due to material property uncertainties or bonding layer compliance.

The state space model thus derived was then further modified to bring it into closer agreement with experimental data. The eigenvalues corresponding to the first three modes were forced to match the experimentally determined frequencies and damping ratios of those modes. Elements in the piezoceramic forcing matrix were changed to produce model transfer functions which better reflected the relative magnitudes of the modes and the zero frequencies. Finally, a single real pole at 4000 Hz was added to the beam model to reflect phase losses measuring approximately 6 degrees at 400 Hz. These losses could be due to lags in the frequency response of the piezoelectric amplifiers and the displacement sensor, and to viscous losses in the epoxy bonding layer between the piezoceramics and the aluminum beam.

The results of these corrections are shown in Figure 4.4, which compares the transfer functions of the original model (before eigenvalue and

other modifications), the corrected model, and the actual beam data. The improvements in the corrected model are such that it is for the most part indistinguishable from the experimental data, except in the region above 700 Hz. This deviation is due to mismodelling of the fourth beam mode at just under 1000 Hz and to the presence of an unmodelled mount mode at about 680 Hz. The relatively low magnitude of these peaks makes the errors negligible under the control scheme to be presented in Section 4.3. The experimentally measured natural frequencies and damping ratios of the first three modes are given in Table 4.1 along with the frequency of the first zero in the control transfer function.

Parameter	Experimental	Basic model	Error
1st modal ω_n	32.57 Hz	31.62 Hz	-2.9 %
2nd modal ω_n	182.04 Hz	177.19 Hz	-2.7 %
3rd modal ω_n	499.14 Hz	489.25 Hz	-2.0 %
1st modal ζ	0.36 %	-	-
2nd modal ζ	0.15 %	-	-
3rd modal ζ	0.20 %	-	-
1st control zero frequency	89.7 Hz	80.6 Hz	-10.1 %

Table 4.1 **Open loop beam characteristics compared to basic model predictions.**

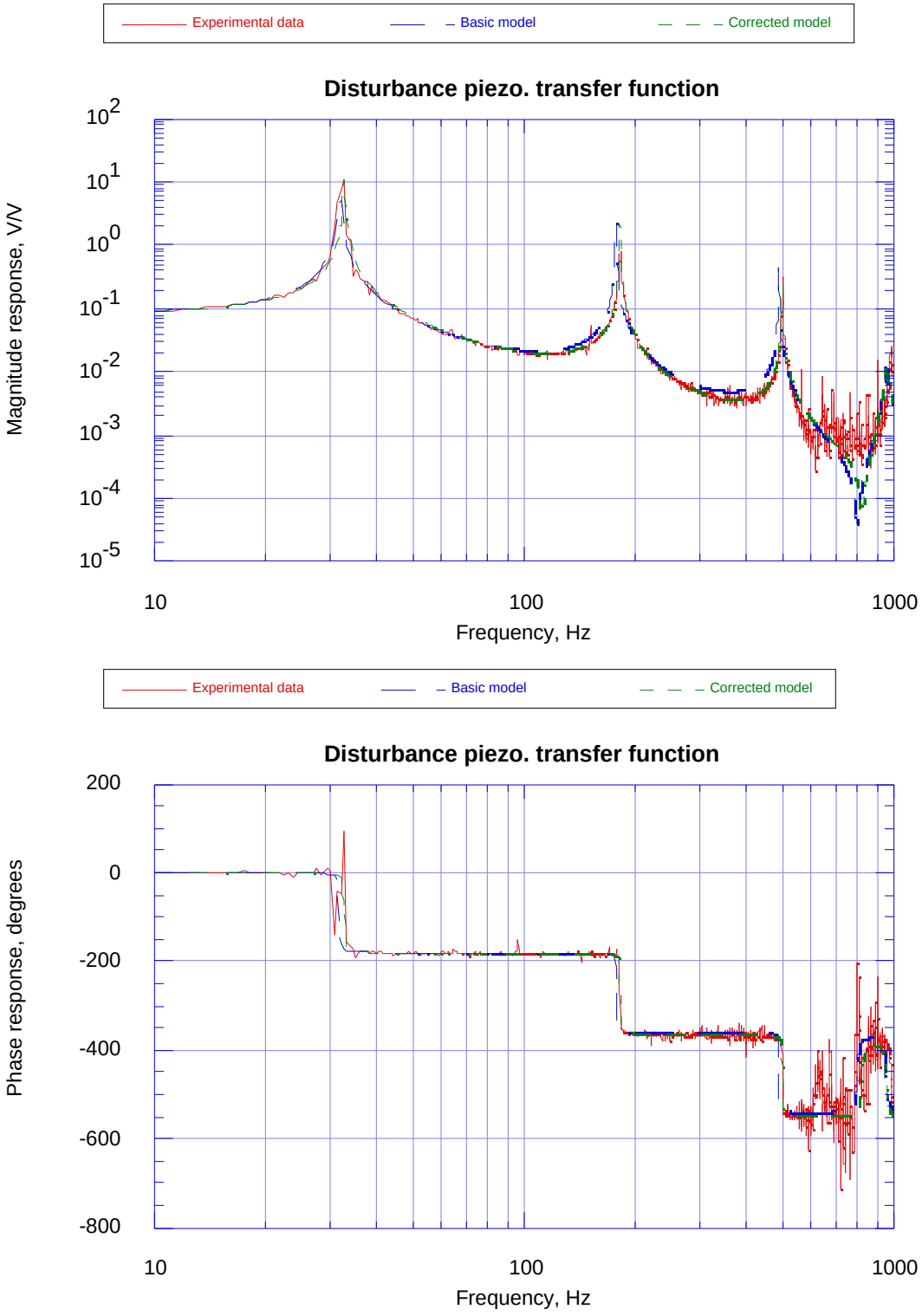


Figure 4.4a **Magnitude and phase of transfer function from signal applied to disturbance piezoceramic pair to signal from tip displacement sensor.**

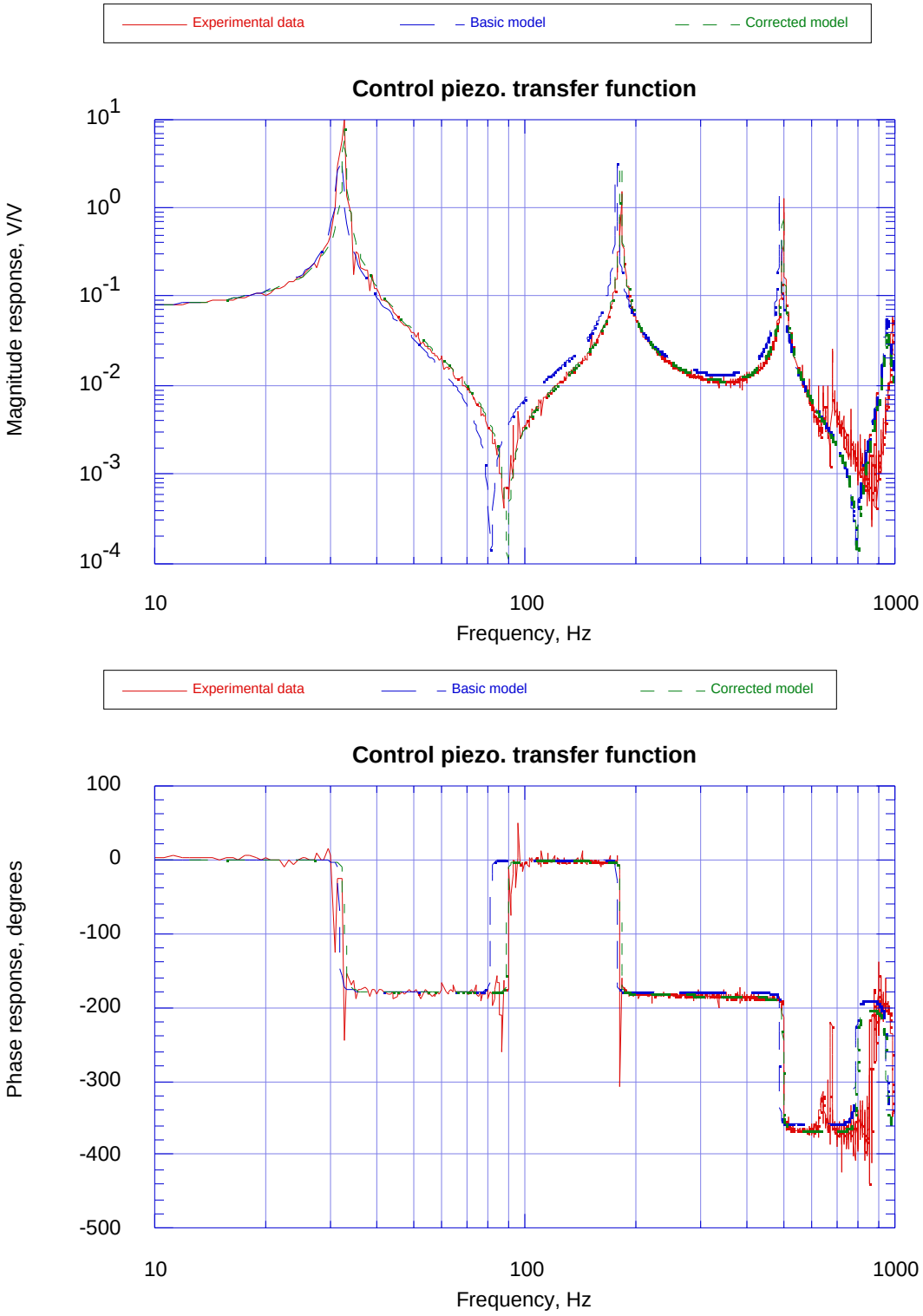


Figure 4.4b **Magnitude and phase of transfer function from signal applied to control piezoceramic pair to signal from tip displacement sensor.**

4.2 Single-chip Microcomputer Controller

As discussed in the introduction to this chapter, the development of intelligent structures with integral control systems favors the use of control processors with functions concentrated on the fewest possible number of chips. The ideal processor would incorporate on a single chip all the varied functional components such as A/D converters, D/A converters, digital communication ports, program and data memory, and the arithmetic and logic unit normally associated with a microprocessor. In addition, the processor must also be capable of performing quick calculations and should easily incorporate input and output operations for real-time control.

The controller for the experiment performed in this work was the Intel ICE-196KB in-circuit emulator, a development tool hosted on an IBM PS/2 which mimics the functionality of the Intel 87C196KB 16-bit high performance CHMOS microcontroller. The 87C196KB was chosen as a representative device having the most complete integration of functions, including substantial analog input and output capabilities, as well as its fast built-in integer arithmetic operations and real-time interrupt capabilities. Although this device is not entirely independent of external chips for support circuitry, it is used to suggest what could be achieved with further specialization and customization. In this section, some of the hardware and software characteristics of the 87C196KB will be described, showing its suitability for use as in demonstration of single chip control capability.

4.2.1 Hardware aspects of the 87C196KB

To begin with, a cursory glance at the constituent elements of a microcomputer is in order. Figure 4.5 illustrates the basic functional components of a typical microcomputer system. The control unit (CU), which directs the execution of program instructions, and the arithmetic logic unit (ALU), which performs elementary operations, together make up the central processing unit (CPU). The main memory contains both random access (RAM) and read-only (ROM) types for storing program instructions and data. A typical microcomputer may also have several different kinds of input and output devices; for a controller, these will likely include provisions for both analog to digital and digital to analog conversions. The serial and parallel communication ports listed are commonly used for interfacing with such I/O devices as CRT screens, keyboards, and mass memory devices such as magnetic or optical disks or magnetic tape; the use of these ports for network communications with other microcomputers could find application in the data exchange necessary for distributed control processing systems.

The basic functions illustrated in Figure 4.5 are performed by integrated circuits on silicon chips. The chips are interconnected by means of conductive paths, or buses, in the boards on which they are mounted. The functions of the CPU are implemented on a single chip called the microprocessor, while each of the other functions generally requires many more chips. For microcomputers (as opposed to supercomputers) the bus lengths are not the primary limitation on speed of operation, so the use of many chips to perform the necessary functions outside the CPU is not a serious problem, although microcomputers have become increasingly more monolithic in the drive for compactness.

The flexibility of the multi-chip architecture of typical microcomputers makes them well suited to the performance of a wide variety of tasks and allows specific implementations of the various functional components to be combined in many different ways. When intended for use as a controller for a structural vibration problem, however, this variety of applications can be sacrificed for simplicity and the consolidation of functions to fewer chips. The input and output devices of a structural controller may be more strictly limited to pre-defined sensors, actuators, and possibly communications with other controllers. The concentration on a single, well-defined task can produce programs of a size which require much less memory than other data processing applications. This specialization and the concurrent simplification can lead to the reduction of many functions to a single chip, as illustrated in the functional schematic of the Intel 87C196KB, shown in Figure 4.6.

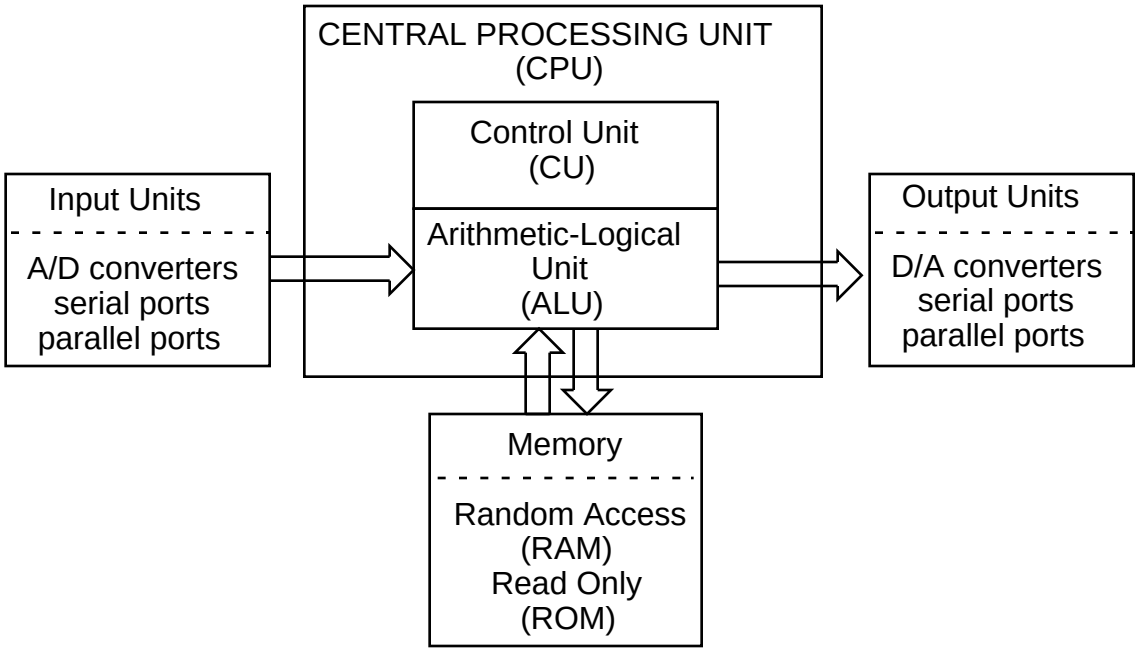


Figure 4.5 **Block diagram of the basic functional components of a microcomputer system. I/O functions listed are typical of a microcomputer used as a controller. (Adapted from [37])**

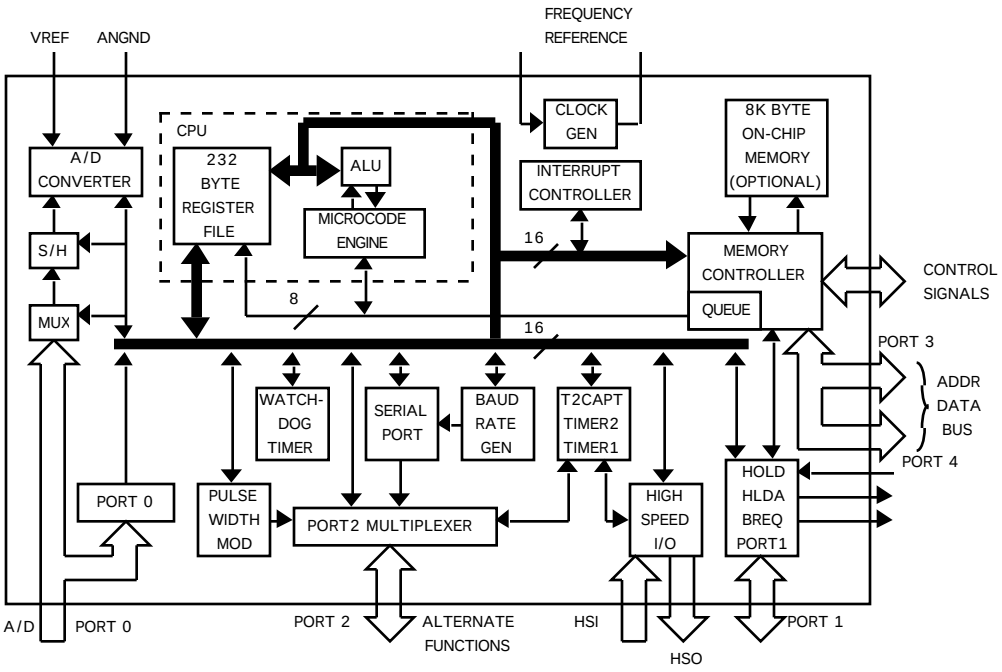


Figure 4.6 Intel 87C196KB block diagram (adapted from [1])

The basic functional components shown in Figure 4.5 may also be identified in the 87C196KB schematic. The I/O devices for this computer consist of 8 10-bit multiplexed analog inputs, 4 high-speed digital inputs, 4 high-speed digital outputs, the 8-bit pulse-width-modulated output, the serial port, and several parallel ports. Memory is also present in the system in the form of the 232 byte register file (RAM) and the 8 Kbytes of erasable-programmable ROM (EPROM). The inclusion of all these elements on a single piece of silicon makes single-chip microcomputers like this one remarkably complete and self-contained, and represents a large step toward the development of embeddable controllers for intelligent structures.

External circuitry required for the operation of the 87C196KB includes, at a bare minimum, both analog and digital +5 V and ground connections and a 12 MHz clock crystal or signal. The power and ground connections are of course indispensable, and could be provided with the clock signal in a

common bus to all processors in an intelligent structure. The analog reference voltage, required for the on-chip A/D converter, could be incorporated on the chip, as in the case of the Analog Devices product AD570 [14].

For use with the displacement sensor and the piezoelectric actuators in this experiment, a few more components are required as shown in Figure 4.1. The inductive element of the displacement sensor had its own signal conditioner which yielded a voltage proportional to the distance between the element and the beam target. Since the beam was free to vibrate, a non-zero offset voltage (approximately -4 V) was present when the beam was motionless. The analog inputs of to the A/D converters require voltage levels between 0 V and +5 V; the input circuit was used to subtract the sensor's inherent offset, amplify the signal, and add an offset of +2.5 V to center the signal in the range of the A/D input. The input circuit had a fixed gain of 16.25 and rolled off to -0.83 dB point at 20 kHz. In a completely integrated intelligent structure, the signal conditioning functions might be implemented on a single chip, possibly on the microcomputer chip itself.

The remaining blocks in the control loop are the elliptic filter and the amplifier to the control piezoelectric pair. The filter was required because the analog output of the 87C196KB is not a nearly continuously varying voltage, but rather a pulse-width modulated (PWM) signal, as illustrated in Figure 4.7. The desired control signal amplitude as determined by the compensator is expressed in terms of the duty cycle of a digital pulse train which switches between 0 V and +5 V and has a frequency of 23400 Hz.

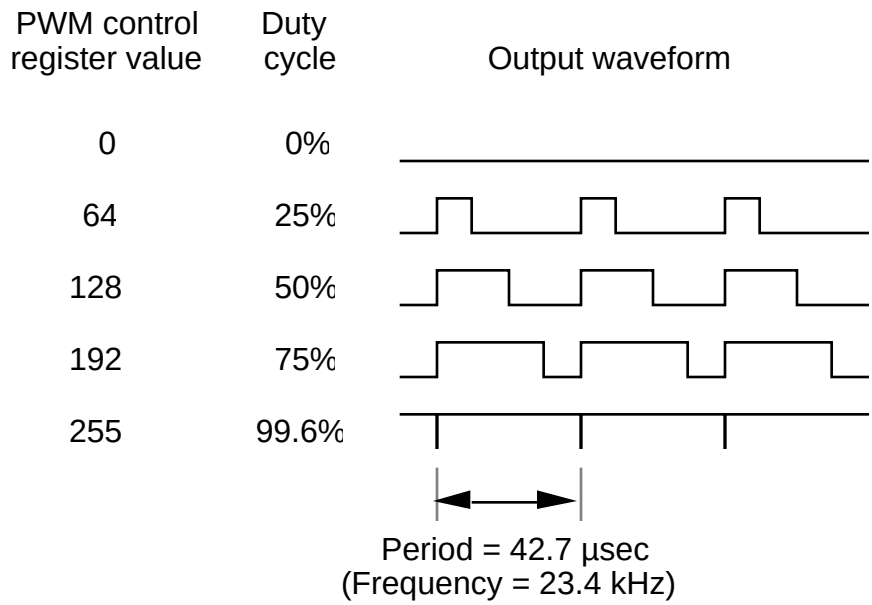


Figure 4.7 **Pulse-width modulation analog output. The desired output level, expressed as an 8-bit number from 0 to 255, is placed in the control register and determines duty cycle, i.e., the duration of the pulse as a fraction of the period.**

In this experiment, a continuous voltage was desired, so that the PWM signal had to be processed through a low-pass filter. A 3-pole elliptic filter was used, the frequency response of which is shown in Figure 4.8 along with that of a mathematical model. The circuit was tuned to place the undamped zeros of the filter at 23400 Hz, the frequency of the major noise component of the PWM signal. The poles of the filter were appropriately placed to provide a -40 dB attenuation ceiling at higher frequencies and a fairly flat response over the frequency range of interest (DC to 1 kHz). Since the PWM signal was limited to 2.5 V excursions about a +2.5 V center, the elliptic filter circuit also incorporated stages to remove the offset and amplify the signal. It was this amplification stage which was used to vary the gain in the control loop.

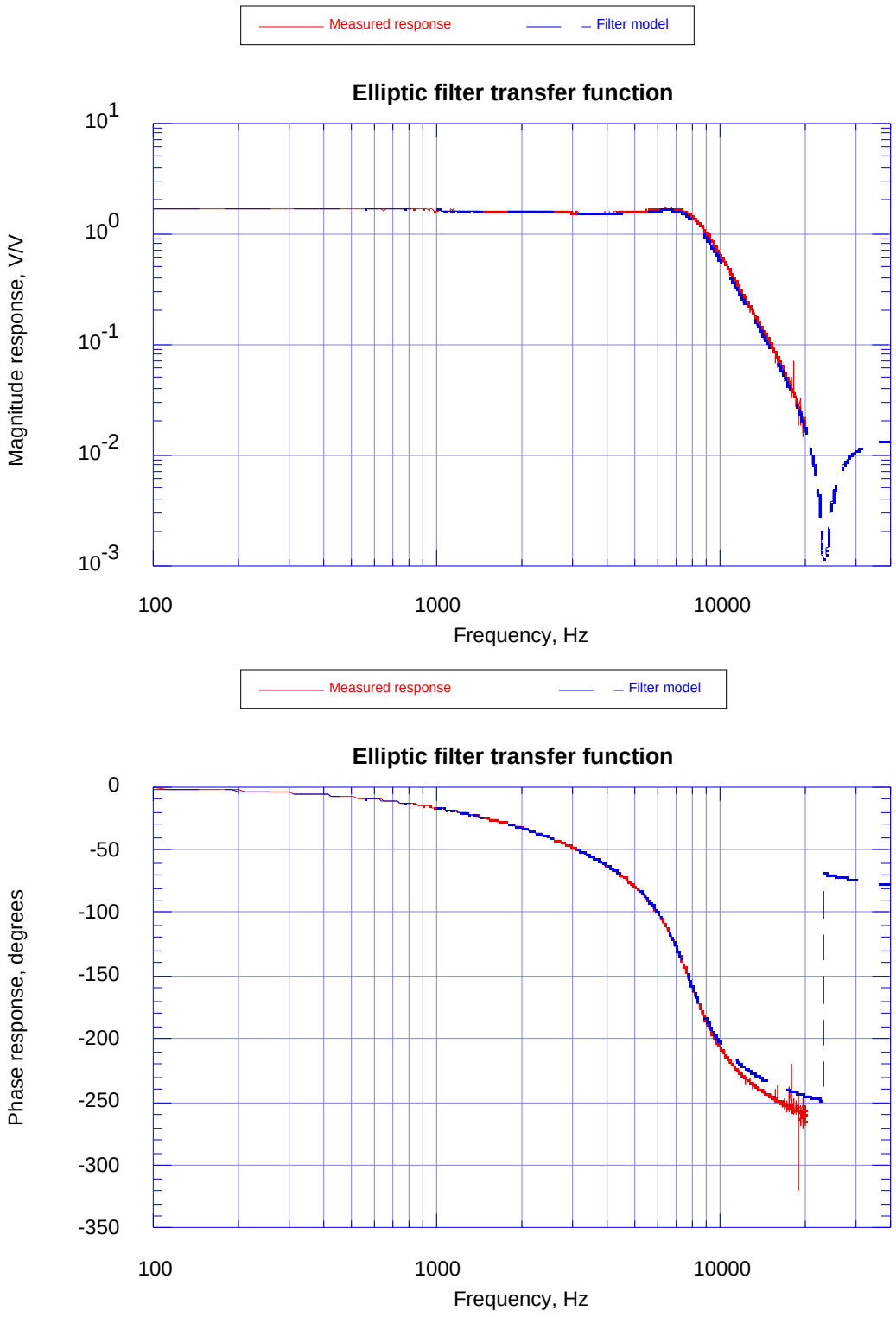


Figure 4.8 **Elliptic filter transfer function magnitude and phase response. Experimental data up to 20 kHz is compared to mathematical model.**

Clearly an integrated intelligent structure would require some other arrangements for output circuitry and power amplification. The elliptic filter with its substantial phase loss could have been omitted had the output of the on-chip A/D been in the more conventional zero-order hold form, but this would still have required an amplifier of the type described in Section 4.1.1. The Apex Microsystems PA08V high voltage op-amps are not well-suited for adaptation to embedding in composite structures. They are hybrid circuits, not monolithic chips; they consist of many separate elements mounted on a ceramic substrate which is bulky compared to a single chip. In addition, any standard amplifier, hybrid or not, will require arrangements for cooling in order to safely drive large capacitive loads at high voltages and frequencies. One possible approach might be to simply use the PWM signal directly to control the state of a low resistance, solid state switch which would alternately apply fixed high and low voltages to the piezoceramic. This would greatly simplify the circuitry and reduce the number of components, and would shift the dissipation from the embedded parts to the main power supply. It remains to be seen, however, how such high frequency switching would be reflected the structural response; presumably the supply output impedance would act with the actuator capacitance to produce a single pole filter at some frequency, but if this effect is too great it would alter the supply voltage levels, preventing the use of more than one actuator with a single power supply.

4.2.2 Programming aspects of the 87C196KB

The single chip microcomputer to be used for control had to be capable of performing its tasks quickly in real time. This required fast built-in arithmetic operations and prompt input-output capabilities. The Intel 87C196KB, with its 0.7 μsec 16-bit additions, 2.3 μsec 16-bit multiplications,

and ability to respond to interrupts, is well-suited to real-time applications.

As mentioned at the start of Section 4.2, the control in this experiment was performed by a development tool, the ICE-196KB, which exactly mimics the performance of the 87C196KB, but is actually a board hosted on an IBM PS/2 microcomputer. The use of the ICE-196KB made the construction of hardware and the development of software more convenient than would have been the case with the actual single-chip device. The PS/2 ran the programs for writing, editing, compiling, and linking the control algorithm source code. It also executed the emulation program which loaded the control algorithm object code into the ICE-196KB memory, and allowed step-by-step debugging and examination of the controller memory and registers during control operation.

Programming the controller was relatively straightforward. The control program was written with Intel's ASM96 assembly language compiler to provide the maximum operating speed and to eliminate the overhead and inefficiencies associated with higher-level languages. Speed was also achieved by the use of integer rather than floating point arithmetic; the processor has fast built-in functions for performing fast 16x16-bit multiplications and 32/16-bit divisions, as well as 16-bit and 32-bit additions and subtractions, whereas the execution of floating point operations would have required the use of external math libraries, decreasing speed and increasing memory usage.

A flow-chart of the control program is shown in Figure 4.9. The control program was allowed to run freely, rather than relying on either an internal or external sampling synchronization signal. The controller was

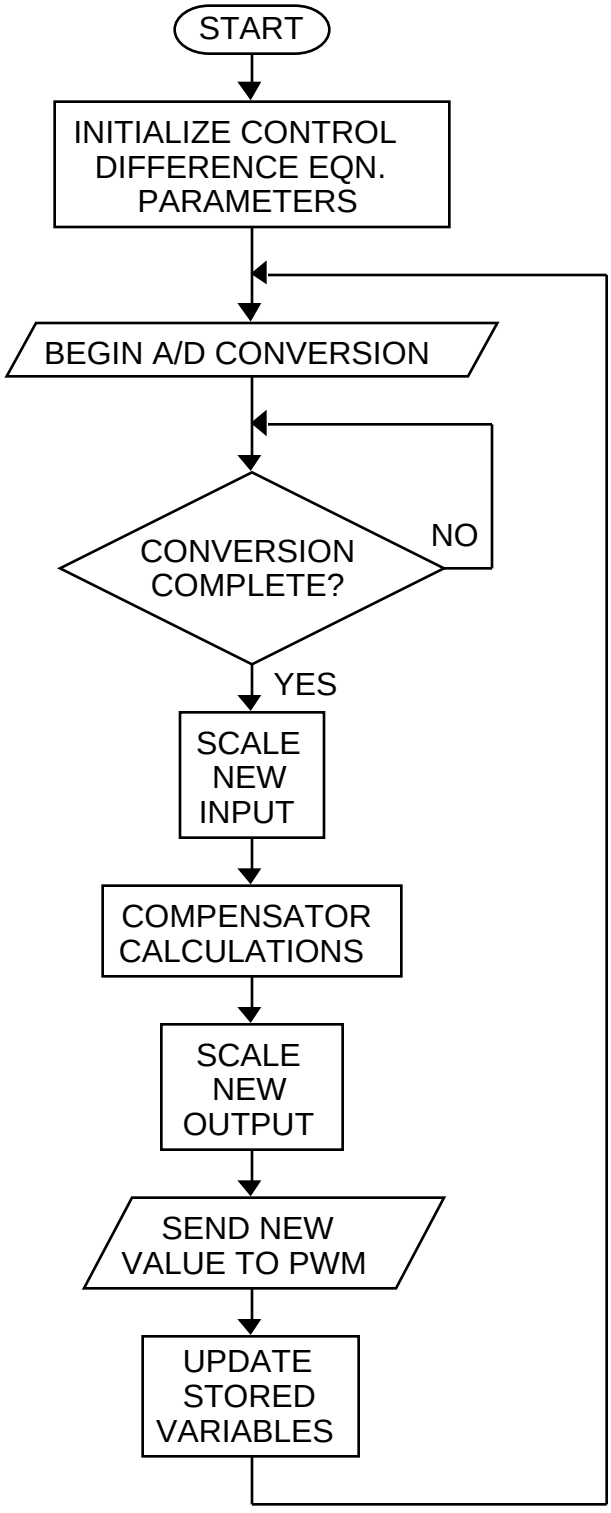


Figure 4.9 **Flowchart illustrating control algorithm program execution.**

interrupt driven, so that after the control parameters are initialized and the A/D conversion was started, the program entered a loop until the A/D conversion function issues an interrupt, signalling conversion completion. Upon receiving this interrupt, the program branched to the code which performed the control calculations and loaded the PWM register with the desired command signal level. The sampling and control loop rate was thus dependent on the time required to perform the A/D conversion and the control computations. The capability exists, however, to adjust the loop execution rate independent of program execution times; the block containing TIMER1 and TIMER2 in the schematic of Figure 4.6 represents a function within the microcomputer which can be used to issue an interrupt at intervals specified by the programmer.

The time required to perform the operations represented by the blocks in the flowchart introduced two significant time delay effects. The first is typical of discrete time control systems which employ a zero order hold to convert a train of output samples to a piecewise continuous function. As illustrated in Figure 4.10, the effect is to delay the signal by half the time interval between successive samples τ_1. It should be noted that the conversion from a continuous to a time-discrete representation requires a knowledge of value of τ_1 in order compute the difference equation parameters needed to correctly map poles and zeros from the Laplace-plane to the z-plane.

The other component additional phase lag of the discrete controller over that associated with the continuous implementation depends on the time delay between a particular input sampling and the corresponding change in the output τ_2. Both of these time delays are illustrated in Figure 4.11, which gives a rough breakdown of the intervals.

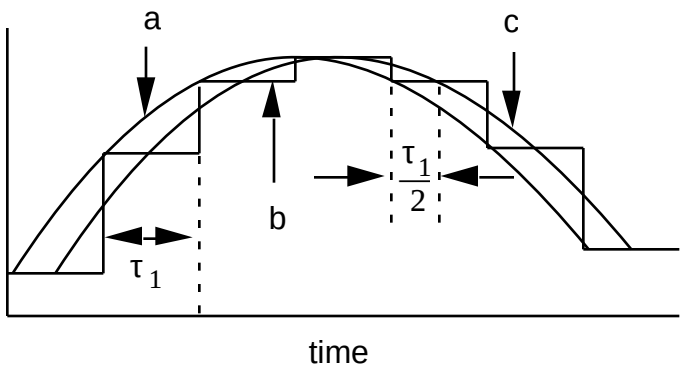


Figure 4.10 **Time delay effect of zero order hold; (a) is the original time signal, (b) is the sampled and held representation, and (c) shows how the zero order hold introduces an effective delay of half the sampling interval.**

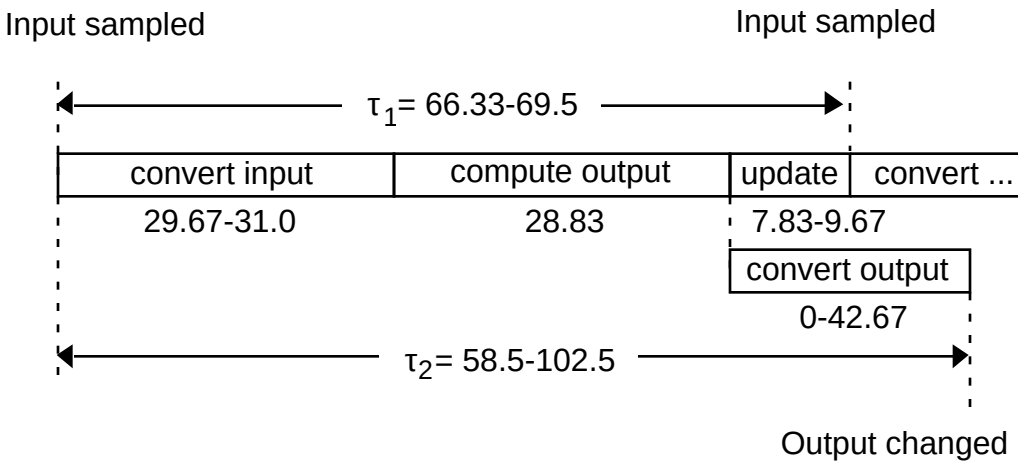


Figure 4.11 **Illustration of the time delays associated with the discrete time implementation of the controller. Times are estimated from tabulated instruction execution durations and are given in microseconds.**

The end result is that the time delay which determines the phase lag of the discrete system with respect to the continuous system is given by

$$\tau_p = \frac{\tau_1}{2} + \tau_2 \tag{4.1}$$

The effects of this delay, along with the phase lag due to the elliptic filter, will prove to be important in the closed-loop behavior of the system, as described in the next section.

4.3 Control Strategy and Implementation

In this section, the compensator used to reject disturbances in the closed-loop system will be described. The control objective may be stated as the desire to use one pair of piezoceramic plates to reject the disturbance of the tip displacement caused by noise applied to the other pair. Since the purpose of the experiment was more to demonstrate the ability of single-chip microcomputer to perform structural control tasks, the control objective was not specified in terms of such usual parameters as phase margin, settling time, or steady-state error. Instead, the performance was simply to be measured by reduction in the RMS level of tip displacement measured over the 0 Hz to 1 kHz band, in the face of a pseudo-white noise applied over the same range.

The choice of compensator form will be explained based on previous experiments with the experimental apparatus and a general control objective. A mathematical model of the compensator, including the effects of the discrete time delay, will be developed and combined with the models of plant components presented in Section 4.2 to produce the predicted closed-loop transfer functions and modal damping ratios.

4.3.1 Selection of the control strategy

The motivation behind the selection of the control strategy used was originally based on an attempt to build on the previous work performed on the apparatus [20]. In that work, attention was focussed on the possible use of passive circuit elements to increase damping within control loops involving piezoceramic actuators. The compensator was designed to be stable at some gain and allow command following, and little else, since presumably the performance effects of changing the passive components within the loop

would be transferrable to other systems and compensators using piezoceramic actuators. Nevertheless, arguments based on classical control and practical experience may be made for the compensator adopted.

As the plant was a lightly damped structure, the energy of vibration would be concentrated near those frequencies corresponding to natural modes. Since the disturbance was to be introduced by white noise through one pair of piezoceramic plates, the open-loop tip displacement spectrum in the presence of white noise would have the same form as the transfer function presented in the magnitude response of Figure 4.4a. In attempting to reduce the RMS value of the tip displacement, it appears reasonable to expect significant success by increasing the damping of the first three modes.

Damping in any given mode may be increased by applying rate feedback to that mode, assuming that the combination of sensors and actuators is such that some measurement corresponding to modal velocity at that frequency is available. The application of this general principle is limited in practice, however, as sensors and actuators generally detect or excite more than one mode, and the phase response may be such that a signal applied with the proper sign at one resonant frequency may have the opposite sign at another, decreasing damping and leading to instability. Furthermore, in cases where only displacement information is available, the rate information must be obtained by differentiation. This can have the disadvantage of amplifying sensor noise at higher frequencies; attempts to attenuate this noise induce additional phase lag. All these considerations come into play when selecting the precise form of a classical compensator.

The magnitude and phase response of the transfer function from the control piezoceramic pair to the tip displacement sensor is shown in Figure

4.4b. It is apparent using a pure differentiator to add 90° to the response would keep the phase above the -180° crossover point until the third mode at about 500 Hz. The absence of a zero between the second and third modes means that a signal intended for rate feed back would have the wrong sign at the frequency of the third mode and would lead to instability when the loop gain at this frequency reached unity. The magnitude effect of a pure differentiator would provide greater amplification at higher frequencies than at lower ones, further aggravating this problem, and possibly causing instability to occur at a higher mode for a lower loop gain. Any attempt to allow higher loop gains (and thus greater damping in the lower modes) by rolling off the differentiator adds to the phase loss problem, especially considering the closeness of the modes.

Some roll-off point is necessary, though; the problem is to find a frequency at which to place it so that the greatest loop gains and attendant damping may be achieved in the lower modes before instability occurs. If the compensator is rolled-off with a double pole between two structural modes with a complex zero pair between them (e.g. between the first and second modes of the control piezo transfer function), the result is the situation illustrated in Figure 4.12. Damping is achieved in mode a, but at the frequency of mode b the feedback has a component of positive rate feedback, so that only very small gains are possible without an encirclement of the critical -1 point by mode b in the Nyquist diagram.

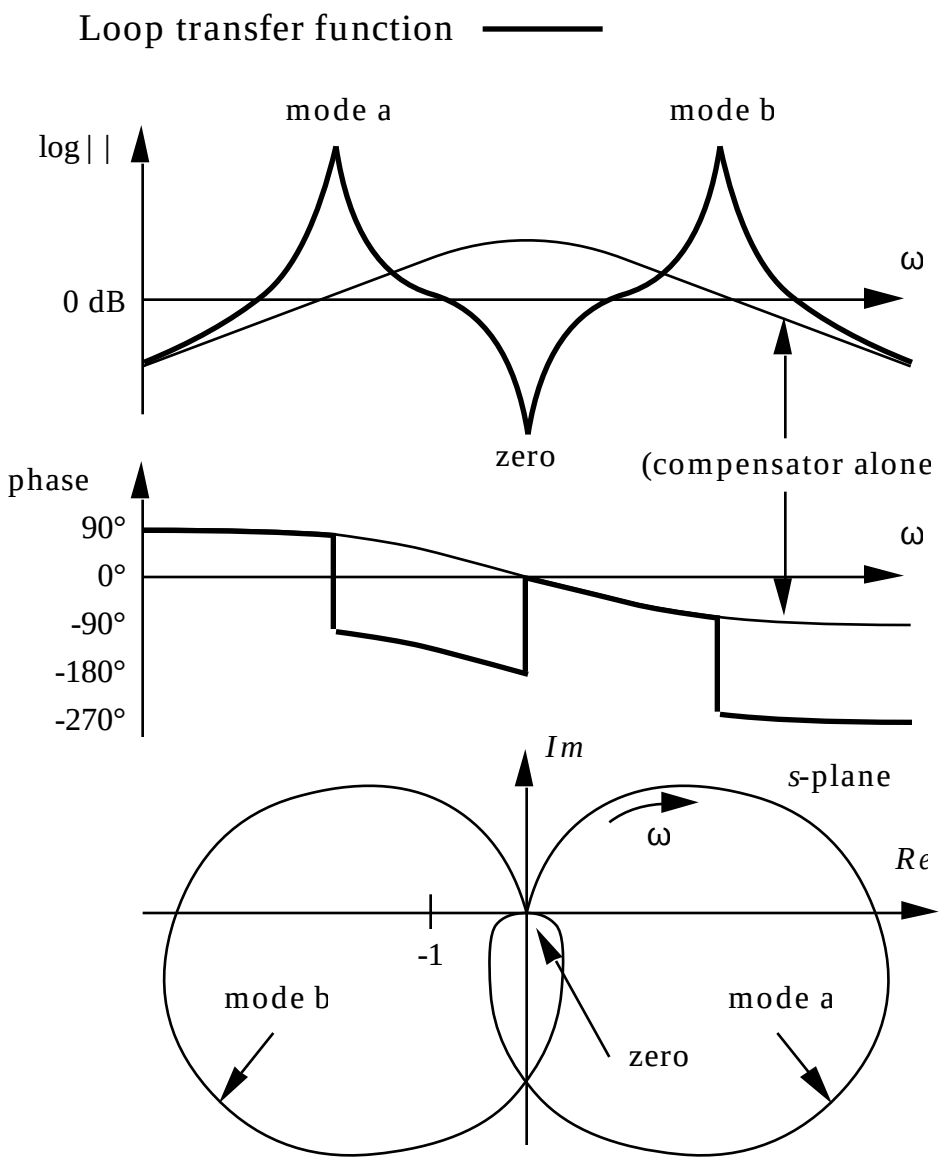


Figure 4.12 **Effects of compensator roll-off between modes with pole-zero alternation shown by magnitude, phase, and Nyquist plots of the loop transfer function.**

If the compensator is rolled off between two modes without an intermediate zero (e.g. between the second and third modes of the control piezo transfer function), the result is the situation illustrated in Figure 4.13. In this case, mode a is again damped, but now the absence of the zeros causes the feedback to have a negative rate component at the frequency of mode b,

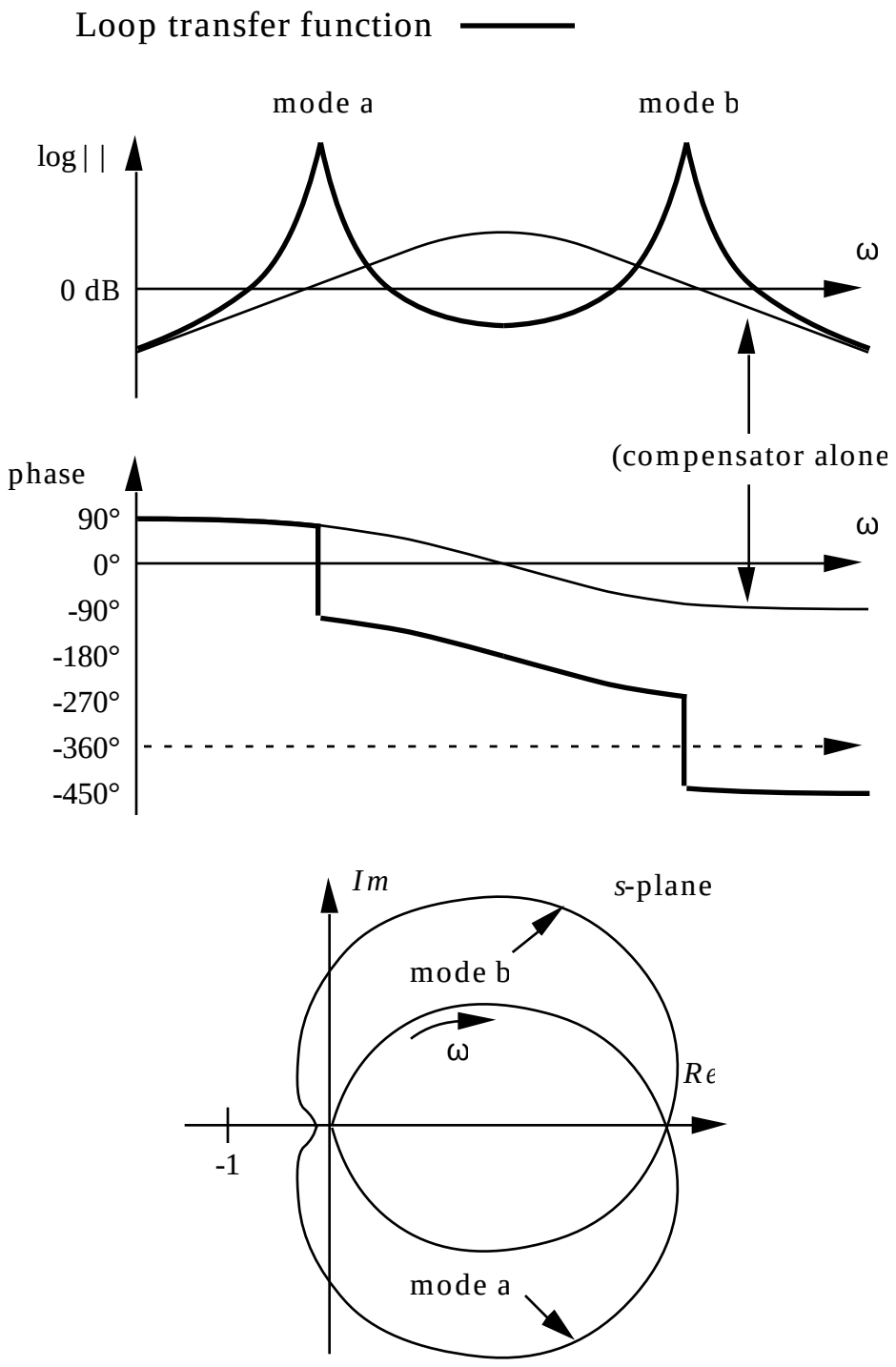


Figure 4.13 **Effects of compensator roll-off between modes with missing zero shown by magnitude, phase, and Nyquist plots of the loop transfer function.**

damping it as well. This is apparent when it is observed that in the phase plot, -360° is the same as 0°. The feedback at mode b also has some component of negative position, which will cause de-stiffening of that mode. Achieving -180° phase crossover at a frequency between the two lightly damped poles where the magnitude response of the loop transfer function is relatively small (though non-zero) means that sizeable loop gains may be applied before encirclement of the critical -1 point in the Nyquist diagram, so that substantial damping of the modes may be obtained.

Thus we have find that a lapse in pole-zero alternation, while destabilizing to pure rate feedback, can be used as a location to place the corner frequency of a rolled-off differentiator, extending its damping effects even to higher modes. Additional phase losses at higher frequencies due to another breakdown in pole-zero alternation or some other cause would tend to be destabilizing, but as frequency increases the attenuation due to the magnitude roll-off of the compensator can be expected to provide some gain stabilization.

The mid-point between the second and third modes on a logarithmic scale is the geometric mean of their frequencies, or about 300 Hz, though the magnitude response of Figure 4.4b shows the actual minimum between the two modes to occur at about 350 Hz. The actual implementation of the compensator will also include the phase losses due to the discrete time and PWM delays, as well as that due to the elliptic filter, which will tend to lower the frequency at which the -180° crossover point occurs. Thus, placing the poles at a still higher frequency, such as 400 Hz, will tend to offset this effect, allowing higher loop gains and increased performance before instability occurs.

4.3.2 Implementation of control

The general control strategy having been determined, a specific implementation must now be developed. This will consist of forming the continuous representation of the compensator, transforming to a discrete time representation, and converting parameter values to actual numbers for use by the single chip microprocessor. The characteristics of the resulting real compensator will be evaluated by comparison with a mathematical model which includes the expected effects of the discretization time delay. Both compensator and loop transfer function comparisons of measured and predicted response will be presented as a final step before the closing of the loop.

The continuous representation of the compensator includes a zero at the origin and two real poles at 400 Hz, which may be written in transfer function form as

$$K(s) = \frac{2bs}{(s+b)^2} \tag{4.2}$$

where b is the pole frequency (2513 rad/sec in this case) and s is the Laplace variable. The coefficient of the numerator was chosen to produce unity magnitude response at the peak frequency.

As mentioned previously, this is similar to the compensator used in earlier work, with the difference that the zero in that investigation was above 0 Hz, providing a non-zero DC gain and the ability to follow commands. A further difference is that the earlier compensator was implemented with an analog circuit; the discrete time compensator requires further manipulation for implementation on a digital computer.

The digital calculations for the compensator were performed in in cascade form; two single pole filters were applied sequentially, reducing numerical precision errors incurred in implementations in which the two are

combined into a single difference equation. This division explicitly introduced an intermediate state in the calculations so that the compensator could be represented as

$$K(s) = \frac{as}{s+b}\frac{c}{s+b} \tag{4.3}$$

Here the gain $2b$ has been divided between the a and c coefficients of the two stages; the proportions of this division were chosen to simplify the discrete representation, as will be shown below.

The continuous transfer function representation of the compensator had to be converted to a discrete time z-transform representation. The trapezoidal or Tustin's Rule transformation which has the advantage over some other transformations that it maps the stable region of the s-plane exactly into the stable region of the z-plane [17]. The Tustin transformation is given by

$$s = \frac{2}{\tau}\frac{z-1}{z+1} \tag{4.4}$$

which, when inserted into the continuous transfer function of Equation (4.3), gives

$$K(z) = \frac{N(z+1)}{z+D}\frac{N(z-1)}{z+D} \tag{4.5}$$

where

$$D = -\left(\frac{1-\frac{b\tau}{2}}{1+\frac{b\tau}{2}}\right) \qquad N = \frac{a\frac{\tau}{2}}{1+\frac{b\tau}{2}} = \frac{c}{1+\frac{b\tau}{2}} \tag{4.6}$$

The two stages of Equation (4.5) may be written in the time domain as difference equations:

$$\begin{aligned} u_{k+1} &= -Du_k + N(e_k + e_{k+1}) \\ v_{k+1} &= -Dv_k + N(u_k - u_{k+1}) \end{aligned} \tag{4.7}$$

where e is the input to the compensator, v is the output, and u is an intermediate state.

The coefficients of these difference equations are the parameters which are loaded at the start of program execution as shown in the flowchart of Figure 4.9. The exact numerical values of the parameters depend on the magnitude of the sampling period τ_1, which, according to calculations based on the time required to perform the operations within the control loop, could be expected to range from 66.33 to 69.5 microseconds. A slightly earlier variation of the control program was used to make experimental measurements of the sampling period; the loop control loop was executed 1024 times, and each time the value of the internal timer (TIMER1 in Figure 4.6) was saved in memory as a 16-bit number. The value in TIMER1 is incremented every 1.333 μsec. Multiplying the difference between the first and last stored times by this interval and dividing by 1024 yielded a sampling period of about 65 μsec, and this value was used for τ_1 in the Tustin transform. The resulting difference equations were

$$u_{k+1} = -(-0.848973259)u_k + (0.373660545)(e_k + e_{k+1})$$
$$v_{k+1} = -(-0.848973259)v_k + (0.373660545)(u_k - u_{k+1}) \qquad (4.8)$$

In order to achieve fast control loop speeds, inputs, outputs, and parameters were expressed as signed integer values. This allowed the use of the quick, built-in integer arithmetic operations available with the 87C196KB instead of the slower floating point routines. Since the A/D and D/A were of 10-bit and 8-bit precision, respectively, the 16-bit integer operations were sufficient to maintain significant digits through the calculations. The decimal values of the parameters in Equation (4.8) were multiplied by $2^{15} = 32768$ (the 16th bit being used to represent the sign) to produce

$$u_{k+1} = -(-27819)u_k + (12244)(e_k + e_{k+1})$$
$$v_{k+1} = -(-27819)v_k + (12244)(u_k - u_{k+1}) \qquad (4.9)$$

These are the values used in the program to implement the compensator calculations. The A/D converter inputs were converted from unsigned to signed integers and scaled so that a full-scale input signal would not cause numerical overflows in subsequent computations. The calculated control output underwent the reverse of this process; it was scaled and converted from a signed to an unsigned integer for loading into the PWM control register. The amount of this scaling and the magnitude of the parameters corresponding to scalar gain were chosen so that a full-scale input signal at 400 Hz, the peak frequency of the compensator, would produce a full-scale output signal. Thus as long as the signal levels were such that the A/D input was within the 0 V to +5 V range, no numerical overflow or output clipping would occur, while at the same time maximum dynamic range would be achieved.

In order to evaluate the fidelity of the compensator frequency response, a mathematical model must be developed. The model compensator consists of three parts: the continuous design, a time delay approximation, and the elliptic filter. The continuous design part is modelled by a zero at the origin and two real poles, but the location of the poles is set to that which would correspond to a system with a time delay midway between the two *a priori* estimates based on instruction execution times, or τ_1 = 67.9 μsec, but using the actual control parameter numbers, which were calculated assuming τ_1 = 65 μsec. This had the effect of placing the poles at (65/67.9)400 = 383 Hz, or slightly lower than the frequency in the original continuous design.

The continuous compensator representation must be supplemented by

an additional phase lag in order to account for the time delay introduced by the time required to perform the conversions and calculations. As developed in Section 4.2.2, this time delay is equal to half the sampling period plus the time between sampling the input and producing the corresponding output. Inserting the upper and lower time delay estimates given in Figure 4.10 into Equation (4.1) we find

$$\tau_{p,\min} = \frac{\tau_1}{2} + \tau_2 = 91.67$$
$$\tau_{p,\max} = \frac{\tau_1}{2} + \tau_2 = 137.25 \qquad (4.10)$$

The effect of this time delay may be modelled by the use of a Pade approximation transfer function [31]. The second order version of this approximation is given by

$$K_p(s) = \frac{\frac{\tau_p^2}{12}s^2 - \frac{\tau_p}{2}s + 1}{\frac{\tau_p^2}{12}s^2 + \frac{\tau_p}{2}s + 1} \qquad (4.11)$$

For comparison with experimental measurements, the model of the computer's function must combine the continuous compensator transfer function with this approximation. Since the elliptic filter is required to turn the PWM output into a smooth signal, the comparison model must also include the transfer function of the elliptic filter as described in Section 4.2.1 and illustrated in Figure 4.8. A comparison of the magnitude and phase responses of the experimental and mathematical compensators is shown in

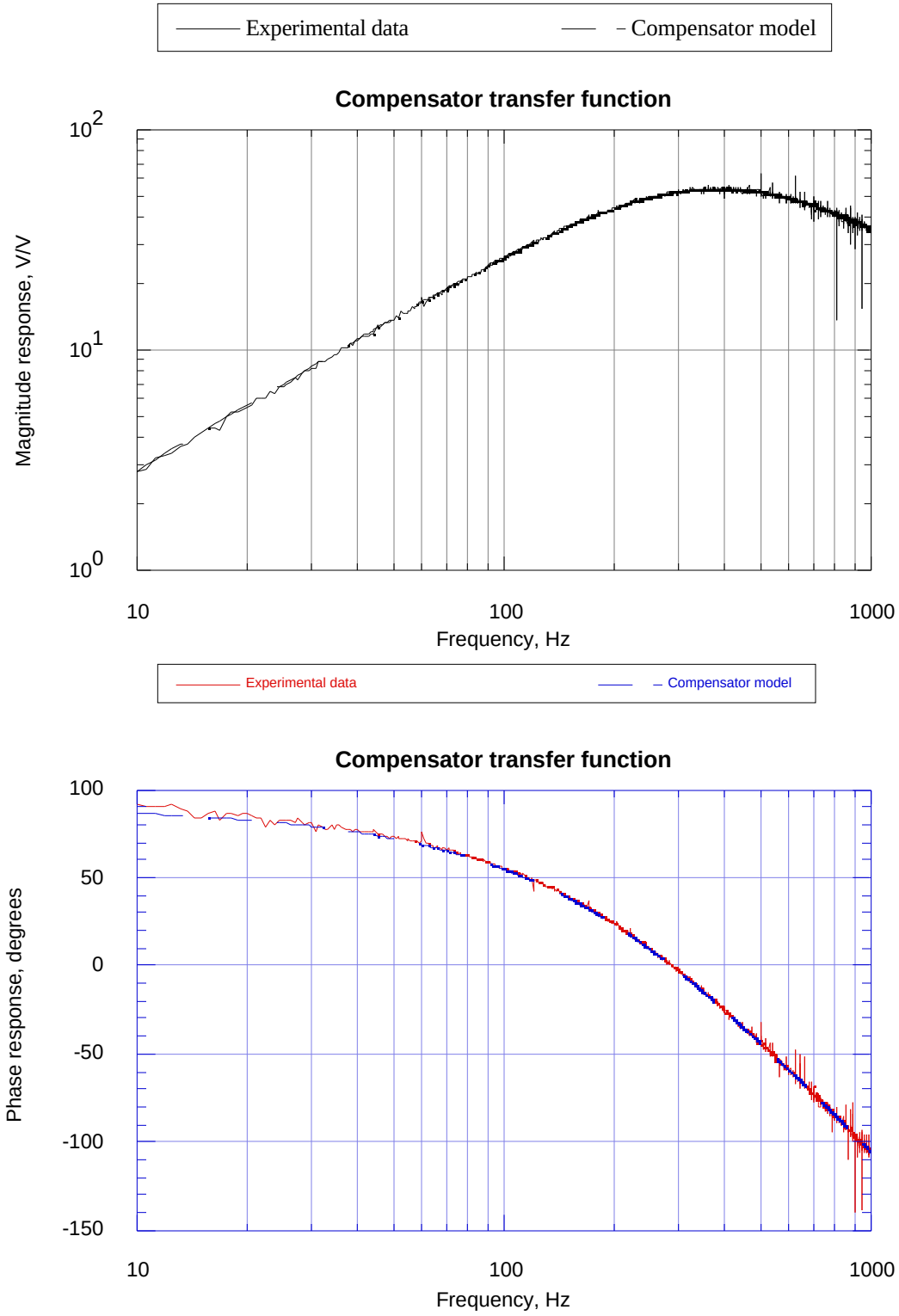


Figure 4.14 **Compensator frequency response. Experimental data is compared to the mathematical model.**

Figure 4.14. The value of τ_p = 114.46 μsec, half-way between the minimum and maximum *a priori* estimates of the sampling period, was used in the Pade approximation. This value produced a model compensator phase response nearly identical to that of the real compensator.

In Section 4.4, the plant and controller models developed to this point are used to predict closed-loop behavior at several gain levels; these results are compared with experimental data. First, though, it is of interest to compare the predicted and experimentally determined loop transfer functions, which consist of combining the compensator (including time delay and elliptic filter) with the beam transfer function taken from the control piezoceramic pair to the tip displacement. The result is the transfer function from the A/D input circuit to the tip displacement sensor signal, as shown in Figure 4.15.

Again, excellent agreement is observed between the model and the experimental data. The point of greatest interest is, of course, the -180° phase crossover point, which occurs at 270 Hz. This is the frequency at which the eventual instability is to be expected as the loop gain is increased. Close examination of the magnitude response reveals that the gain is 0.75 at this frequency. Since this transfer function corresponds to an elliptic filter gain setting of 1.65, the instability should occur when the elliptic filter gain is increased to 2.20. It is difficult to tell from these plots whether the second or third mode is the one which will eventually become unstable, but the phase response shows a sensitivity to lags; a 3° change in phase would correspond to roughly a 10 Hz shift of the -180° phase crossover frequency. It should be noted that the elliptic filter and the time delay alone contribute 6.8° and 6.6° degrees of lag at this frequency, respectively.

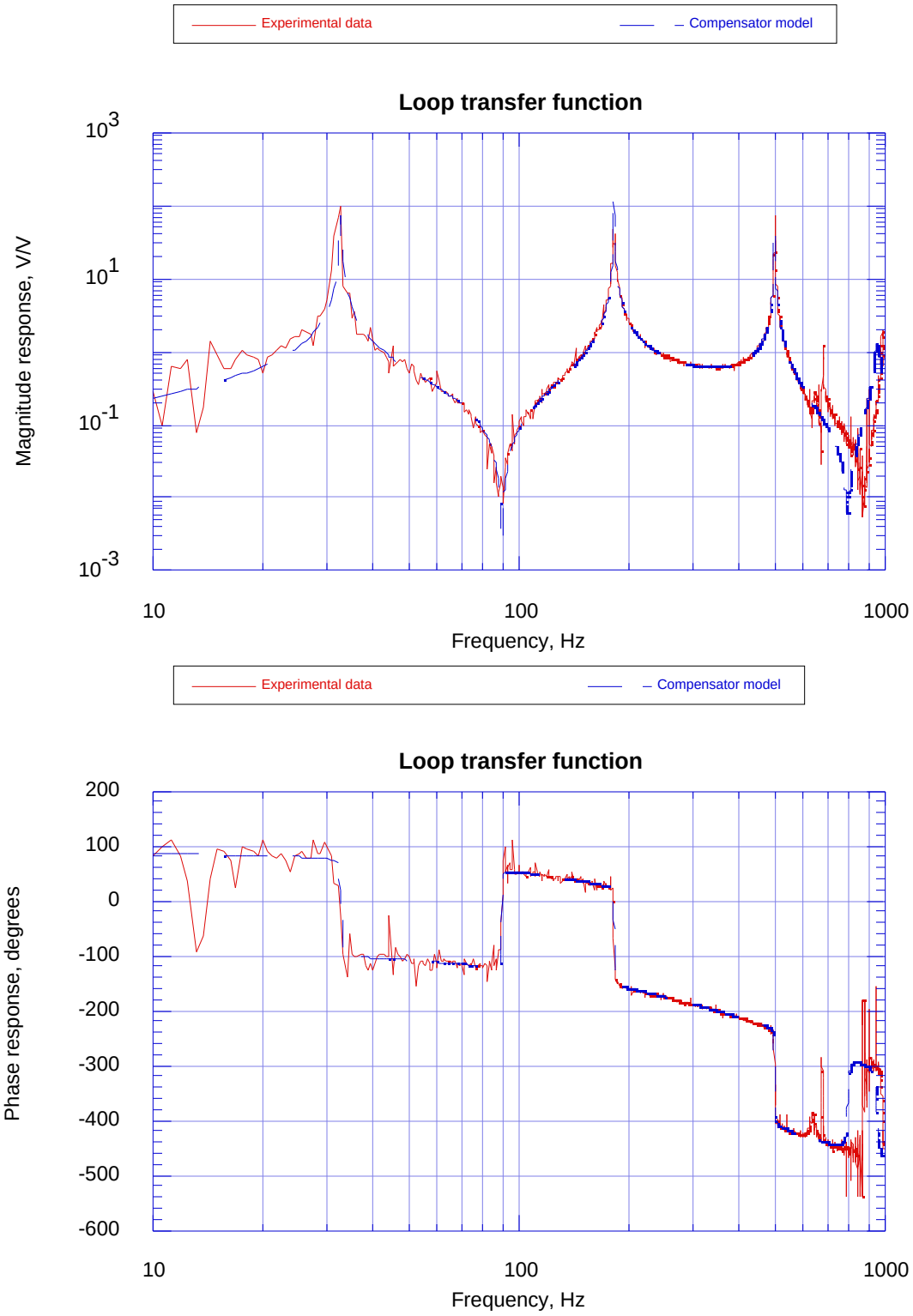


Figure 4.15 **Loop transfer function. Experimental data is compared to the mathematical model.**

4.4 Model Predictions and Experimental Results

In this section, the results achieved in the closed-loop control experiments will be presented along with the corresponding model predictions. The behavior of the system at several loop gains will be described. Data will be presented in the form of transfer functions, root loci, and measurements of pole frequencies and damping ratios and RMS noise attenuation measurements.

4.4.1 Experimental procedure

The basic experimental setup is shown in Figure 4.1. This illustrates the arrangement of plant, control components, and the data gathering equipment used for obtaining the open and closed-loop transfer functions. The output function of the Tektronix 2630 Signal Analyzer was used to produce a burst of pseudo-random noise over the frequency band from 0 Hz to 1 kHz. This noise was applied to one piezoceramic pair to introduce the disturbance to be rejected. The Tektronix analyzer used this signal as a trigger to synchronize the recording of the signal from the tip displacement sensor. The time traces thus obtained were used to produce the transfer functions from the disturbance to the tip displacement.

As mentioned in Section 4.2.1, the gain setting of the elliptic filter was used to vary the control loop gain. Since the loop transfer function had a zero at the origin, the DC gain level was zero. The value of the elliptic filter gain will be used instead to identify the different control gain levels. The initial selection of gain setting was made by exciting the disturbance piezoceramic pair with a constant level of pseudo-random noise over 0-1 kHz and observing the RMS value of the tip displacement signal as computed by the Tektronix analyzer over the same frequency band. The elliptic filter gain was

then adjusted until the greatest attenuation of the disturbance was observed. Transfer function and pole ring-down data were then gathered at that gain level, as explained below in this section. Four other gain levels were tried as well to provide more points for comparison with the model, so that six sets of data were gathered in all, including the open-loop measurements.

Each transfer function was based on 32 time averaged traces of disturbance noise and response. This was made possible by the pseudo-random nature of the disturbance; since the disturbance was repeatable, any response to external noise effects would tend to be averaged out. This yielded sharper magnitude and phase responses than could be obtained by taking the average of a number of transfer functions each based on a single pair of time traces.

At each gain level, an attempt was made to identify the closed-loop frequency and damping ratio of the three lowest modes. The burst random input was replaced by a sinusoidal signal from a Wavetek Model 191 function generator. The Wavetek was operated in a gated mode; an external square wave with a variable frequency was used to produce sinusoidal bursts of sufficient length to produce a steady state excitation, interspersed with periods of dead time sufficient to allow a substantial amplitude decay to be observed. The frequency of the Wavetek was adjusted until a peak steady-state response was observed. Ten time traces of the tip displacement decay were then recorded with the Tektronix analyzer, using the external square wave as a trigger. Due to a slight variability in the square wave frequency, the set of time traces thus obtained for a particular mode and gain level could not be averaged; instead, each trace was separately analyzed to identify the modal parameters.

The open-loop modes were sufficiently lightly damped so that a simple fit of an exponential envelope to the oscillation peaks and a count of zero crossing together provided a good measure of the damping ratios natural frequencies. In the closed-loop tests, however, this method was not practical, since in some cases the decay occurred so quickly that only a few oscillations were distinguishable, while in others the contributions of lower modes were noticeably present in the data. In order to extract the characteristics of the mode of interest from these tests, a decaying sinusoid curve fit was performed on the data using the Nelder-Meade simplex algorithm provided in MATLAB by Math Works, Inc. The curve parameters included the frequency, damping ratio, amplitude, and phase of the mode in question, as well as the amplitude and phase any lower modes, the frequency and damping ratio of which had already been computed. Figure 4.16 shows a sample of ring down data in which some contribution from the first mode is present in what is meant to be a test of the second mode. As is apparent from the comparison, the curve fit successfully accounts for this effect, allowing the desired second mode parameters to be extracted. This procedure was not effective for all modes and all gains, however; at the two highest gains the third mode was no longer discernable, and at the highest gain, excitation of the second proved difficult since the system was close to instability.

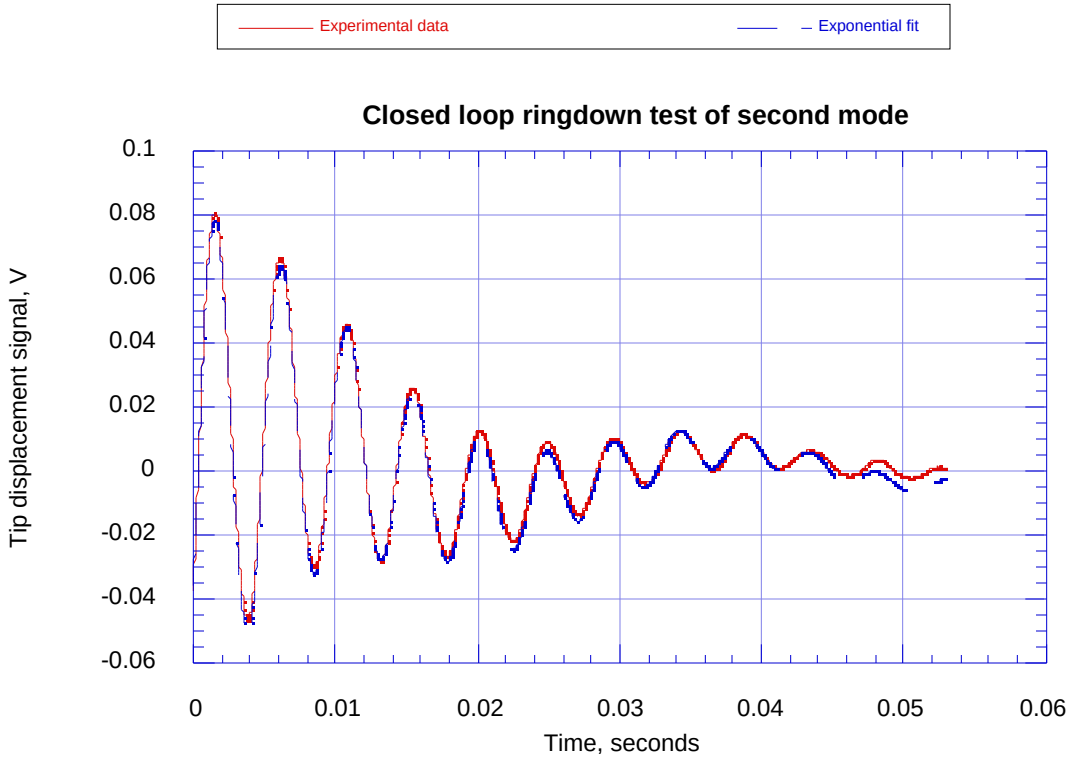


Figure 4.16 **Time trace of ringdown from sinusoidal excitation of second mode and exponential fit used to identify modal frequency and damping ratio. Note component of first mode included for better fit.**

4.4.2 Closed loop response

The behavior of the closed-loop system can be characterized and displayed in many different ways. In this section pole-zero diagrams will be presented illustrating the structure of the open-loop system, followed by a root locus showing the movement of some of the structural poles as the control gain is increased. A comparison between the model and the experimental pole natural frequencies and damping ratios is also presented in the form of a table. Closed loop transfer functions are plotted for several gains, and finally the model and the experiment are evaluated in terms of the original control objective: attenuation of the disturbance response over the 1 kHz frequency band.

Figure 4.17 gives an overview of the pole-zero structure of the open-loop system. This shows the contributions of the various components of plant and controller to the loop transfer function. In addition to the pure imaginary zeros and the poles of the elliptic filter, this view also shows the relative locations of the poles and zeros of the Pade approximation of the time delay, the real pole added to the beam model as mentioned in Section 4.1.2, and the zeros which are placed symmetrically about the imaginary as well as the real axis. Experience has shown that these last are typical of truncated mathematical models of structures.

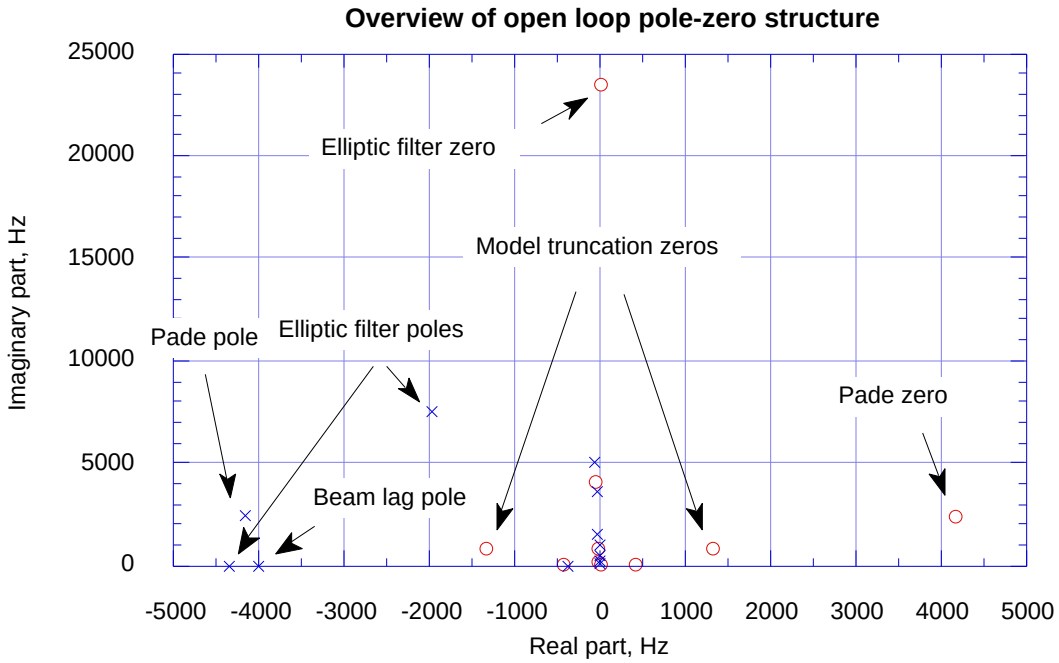


Figure 4.17 Open loop pole-zero structure overview.

Figure 4.18 shows an enlarged view of the pole-zero structure in the frequency range of interest. In addition to the poles and zero of the compensator and the lightly damped poles and zeros of the beam, two additional real zeros appear symmetrically about the imaginary axis. These

may be attributed to the non-collocation of the sensor and actuator pair [16]. It is interesting to note that for this system the non-minimum phase aspect introduced by non-collocation is significant at a much lower frequency than that due to the time delay as represented by the Pade approximation.

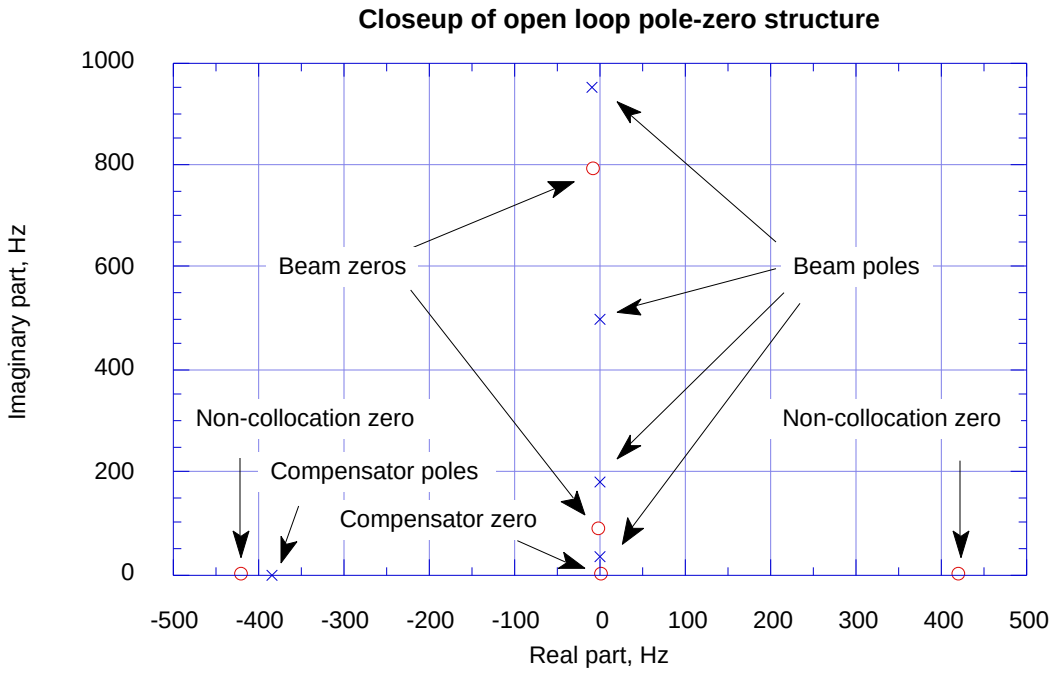


Figure 4.18 Open loop pole-zero structure overview and closeup.

Figure 4.19 presents the results of the experimental identification of pole positions along with the predicted model zero locations and root locus pole trajectories. This shows good agreement between the model and the experiment to the extent that the closed-loop poles could be identified. The first, third, and fourth modes show almost pure damping, while the second exhibits damping and stiffening before going unstable.

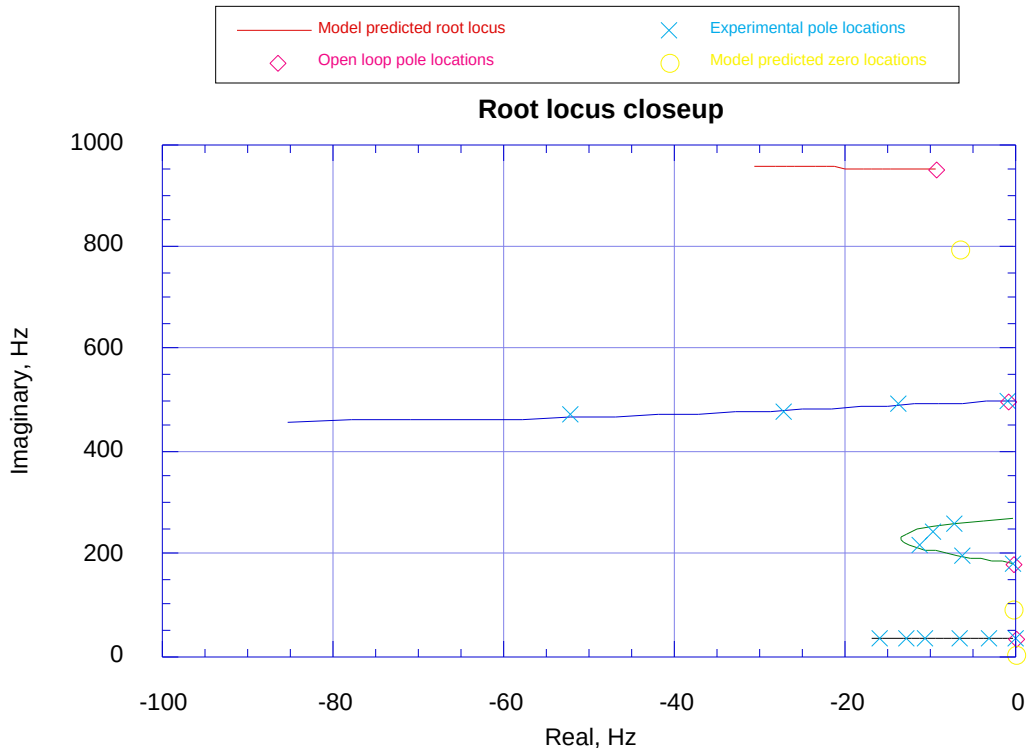


Figure 4.19 **Root locus showing predicted and experimentally determined motion of first four structural poles.**

The same information on pole locations is presented in tabular form as natural frequencies and damping ratios of the first three modes in Table 4.2. The complete range of measurements was only possible for the first mode; as the gain was increased, the magnitude peak of the third mode became impossible to distinguish, and near instability, bounded excitation of the second mode became increasingly difficult.

Another display of the closed-loop behavior at different gains is shown in Figure 4.20. The magnitude response of both the model and the experimental system are presented. The damping of the first and third modes is apparent, as is the damping, stiffening, and undamping of the second mode. The fourth mode can be seen to be slightly damped in the model responses, though this is difficult to distinguish in the experimental data.

Mode No.	Gain	Predicted		Actual	
		ω_n, Hz	ζ, %	ω_n, Hz	ζ, %
1	0.00	–	–	32.6	0.36
	0.55	33.37	10.30	32.8	9.7
	1.08	34.44	20.17	33.8	19.4
	1.65	36.10	31.28	35.0	30.5
	2.01	37.62	38.67	37	35
	2.19	38.60	42.50	38	42
2	0.00	–	–	182.0	0.15
	0.55	195.85	3.25	195.9	3.14
	1.08	214.23	5.52	215.0	5.2
	1.65	241.13	5.25	242.0	4.0
	2.01	260.13	2.51	258.0	2.8
3	0.00	–	–	499.1	0.20
	0.55	489.28	2.87	490.9	2.78
	1.08	479.26	6.23	480	5.7
	1.65	469.38	11.25	473	11

Table 4.2 **Closed loop pole frequencies and damping ratios at several elliptic filter gains as predicted by the model and as measured. Measured open-loop locations are included for comparison.**

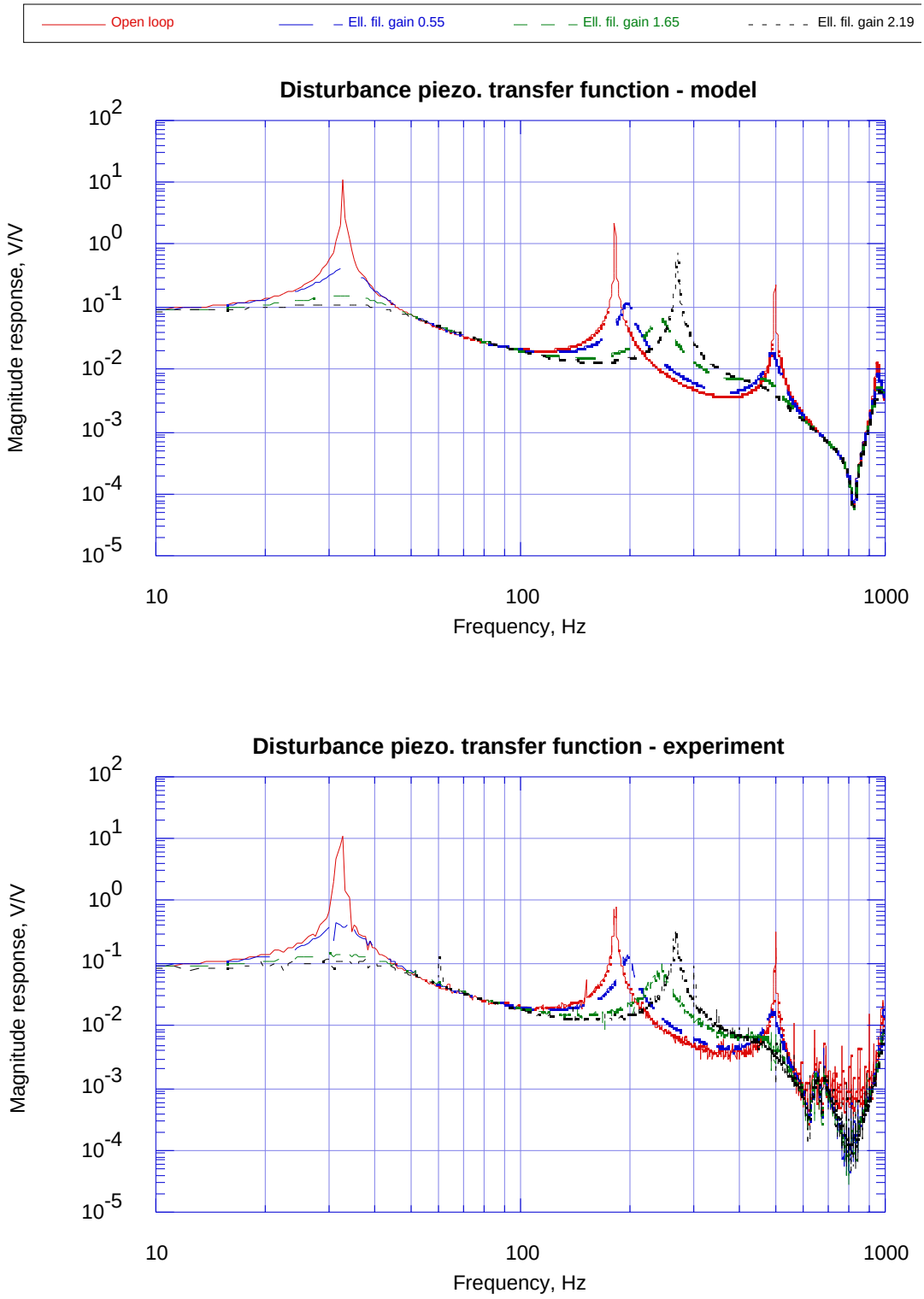


Figure 4.20 **Closed loop response to disturbance at four gains - mathematical model and experimental data. Open loop included for reference.**

Finally, a comparison of the model and experimental performance in terms of the original design objective is given in Figure 4.21. It was stated in Section 4.3 that the purpose of the controller was to reduce the RMS tip response to a broadband noise input to the disturbance piezoceramic pair. The RMS response can be calculated from the frequency response according to the formula

$$RMS(y) = \sqrt{\lim_{T \to \infty} \frac{1}{T} \int_0^T y^2(t)dt} = \sqrt{\lim_{\omega \to \infty} \frac{1}{2\pi\omega} \int_0^{\omega} Y^2(\nu)d\nu} \qquad (4.12)$$

where Y is the magnitude of the Laplace transform of the time domain quantity y. If the input is pure white noise, Y is the same as the magnitude of the transfer function. The Tektronix analyzer measured the transfer functions at 1601 evenly spaced discrete frequencies over the band 0 - 1 kHz, so the second integral in Equation (4.12) could be replaced with a summation to give

$$RMS(y) \approx \sqrt{\frac{1}{2\pi(1601)} \sum_{i=1}^{1601} Y^2(\nu_i)} \qquad (4.13)$$

This approximation was applied to the transfer functions measured experimentally and to those predicted by the mathematical model. The results are presented in Figure 4.21. Both the predicted and experimental RMS levels are normalized by the predicted RMS level for the open-loop system and plotted as a function of the elliptic filter gain. The model and experiment show fairly close agreement except for the open-loop case and the highest gain level. This discrepancy may be attributed to the difficulty of obtaining precise experimental amplitude measurements in the vicinity of lightly damped modes. Since the resolution of the analyzer was fixed, the high sharp peaks were not accurately reflected in the data, introducing error in the summation, while the model transfer functions contained no

measurement error. This was the rationale for normalizing the computed RMS values by the open-loop value obtained from the model rather than by that found experimentally. The results show a maximum disturbance response attenuation of slightly more than 20 dB for an elliptic filter gain of 1.85, which is some 85% of the gain at which instability occurs.

Figure 4.21 **RMS attenuation of disturbance as a function of elliptic filter gain.**

In this chapter we have seen that a commercially available microcomputer exists which is capable of performing real-time structural control tasks, and which contains on a single chip functions which are normally implemented on many chips. Because of the general-purpose nature of the microcomputer, some external circuitry was required, but there appears to be no compelling reason why much of this could not also be

implemented on a more specialized single-chip microcomputer. Such an advanced device might well be capable of performing the tasks envisioned for a local controller in a hierarchic control system such as that described in Chapter 2, as well as being suitable for embedding within a structure by means of the technique presented in Chapter 3. A fully integrated intelligent structure would then be realizable.

CHAPTER 5:
CONCLUSION

The purpose of this report was to explore the possible advantages and feasibility of physically embedding electronic components for the control of intelligent structures. This was approached from three perspectives. First, the effects of distributing the components required to implement the functions of the control system were examined in terms of computational load as well as numbers of required chips and communications lines. The issues involved in physically embedding electronic components in graphite/epoxy composite structures were then addressed, a technique for embedding was developed, and the resulting specimens were subjected to mechanical and environmental tests. Finally, a single-chip microcomputer was used to illustrate the capability of the devices which could possibly be embedded.

In Chapter 2 it was found that for a structure equipped with a large number of sensors and actuators, signal quality over long leads might be improved by distributing signal conditioning circuitry at the transducer locations. A reduction in the number of communications lines leading out of the structure from $O(n)$ to $O(\log_2 n)$ could be achieved by implementing a digital bus system, requiring the distribution of A/D and D/A conversion functions as well as the digital bus interface.

Increasing the degree of distribution to include some digital control processing, faster control loop speeds could be achieved through the implementation of a hierarchical control algorithm. In such an algorithm, model reduction for the control of global deformations and block

diagonalization of the control of the local deformations are used with parallel processing at the local level to produce control loop periods with an $O(n)$ dependence on system size, as compared to the $O(n^2)$ dependence of a traditional centralized system. A high local to global loop speed ratio could also be used to better match the speeds of the loop to the frequencies of the deformations they control.

The feasibility of embedding electronic components in intelligent structures was established in Chapter 3. A technique for embedding integrated circuits with TAB packaging inside graphite/epoxy laminates yielded test articles which survived the composite cure cycle with functioning devices. In mechanical load tests the embedded electronics performed well above usual structural design load limits, and in some cases up to complete laminate failure. The presence of an RTV protective layer was shown to be highly effective in preventing mechanical load transfer to the embedded device. The electronic failure mode was identified to be open circuiting due to weakness in the bonds of the copper leads to the chip and cracks in the leads themselves.

When subjected to a moderately long 125 hour temperature-humidity-bias test, embedded devices survived for durations varying from 14 hours up to the limit of the test. Deviations from nominal behavior of specimens were indicative of corrosive damage to the leads or lead bonds. Direct post-test inspection of the embedded devices supports the conclusion that, as in the mechanical tests, the leads and bonds were most likely to be the critical weakness in the THB tests.

In Chapter 4, a commercially available single-chip microcomputer was shown to be capable of performing a simple control task with relatively little

extra circuitry. The tip displacement disturbance response of a cantilever beam with piezoelectric actuators was reduced by 20 dB from the open-loop level, and damping ratios of 31%, 4%, and 11% were achieved in the first three modes, demonstrating a substantial degree of control effectiveness. This achievement, together with the other functions present on the chip, support the conclusion that with a still greater level of functional integration, leading to a further reduction in the number of components and increased suitability for physical embedding, such a device or a near derivative might well be able to perform as a local controller in the hierarchic control architecture of an intelligent structure.

On the basis of the work described in this report, the preliminary conclusion may be drawn that physically embedding electronic components for the control of intelligent structures is both advantageous and feasible. A distributed processor system has been shown to yield benefits in terms of signal quality, ease of connection, and control system speed. The ability to actually embed electronic components has been successfully demonstrated. Furthermore, the plausibility of the development of custom designed components suitable for embedding and capable of performing required control functions has been established.

In view of the results of this preliminary feasibility study, several profitable directions for the future development of intelligent structures with embedded electronics are indicated. These include extensions of the work addressing the issues surrounding physical embedding as well as the work regarding the implementation of distributed processing schemes such as hierarchic control.

Based on the results of the embedding experiments, one obvious next

step would be to manufacture devices with heavier leads and more robust bonds. Further work could also be performed on the development of the mechanical isolation layer, especially with regard to the effectiveness of such an RTV layer in a THB test. More analytical effort should be devoted to the modeling of the load transfer and composite fracture mechanisms, as well as the effects of varying ply numbers and orientations and loading configurations. This would involve calculation of the strain field in the vicinity of the device due to the far field load; appropriate fracture models for inclusions and free edges could be applied to assess laminate strength. In addition, the fatigue and fracture performance of the embedded devices could be investigated by modeling of the strain state in the device and its interconnections. The electrical and chemical impact of the laminate fibers and resin on the embedded devices could also be studied more thoroughly. Finally, experiments similar to the ones described in Chapter 3 should be performed on a much larger number of specimens in order to provide a statistical foundation for quantitative as well as qualitative comparisons with analytical predictions.

In addition to ruggedizing the devices and building up the theoretical understanding of embedding electronics, a further programmatic step in the development of intelligent structures could be the demonstration of simple specimen incorporating a sensor, an actuator, and some level of processing in a single part. This step would entail the development of custom micro-devices capable of both performing useful functions (unlike the device in Chapter 3) and being embedded (unlike the controller in Chapter 4). A structure with fully embedded closed-loop control might be preceded by an intermediate step involving the embedding of a single sensor or actuator transducer along with relatively simple analog circuitry (i.e., signal

conditioning or amplification).

Another possible direction for future work might be the application of a distributed control scheme with a structure with integrated and functioning, but not embedded, processors and signal and power conditioning electronics. This could be used to validate analytical predictions regarding the performance of such algorithms as the hierarchic one described in Chapter 2, as well as to demonstrate their implementation in actual hardware. Such work would entail more concrete definition of the computational and communications requirements of local and global processors. The development of such a system would represent another important intermediate step in the development of a full up intelligent structure.

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